Simulation Methods For Esd Protection Development By Harald Gossner

Electrostatic Discharge is a pervasive issue in the semiconductor industry affecting both manufacturers and users of semiconductors. This easy-to-read, practical handbook presents an overview of ESD as it effects electronic circuits and provides a concise introduction for students, engineers, circuit designers and failure analysts.

Electrostatic discharge (ESD) continues to impact semiconductormanufacturing, semiconductor components and systems, astechnologies scale from micro- to nano electronics. This bookintroduces the fundamentals of ESD, electrical overstress (EOS),electromagnetic interference (EMI), electromagnetic compatibility(EMC), and latchup, as well as provides a coherent overview of thesemiconductor manufacturing environment and the final systemassembly. It provides an illuminating look into the integration ofESD protection networks followed by examples in specifictechnologies, circuits, and chips. The text is unique in covering semiconductor chip manufacturingissues, ESD semiconductor chip design, and system problemsconfronted today as well as the future of ESD phenomena andnano-technology. Look inside

for extensive coverage on: The fundamentals of electrostatics, triboelectric charging, andhow they relate to present day manufacturing environments ofmicro-electronics to nano-technology Semiconductor manufacturing handling and auditing processing toavoid ESD failures ESD, EOS, EMI, EMC, and latchup semiconductor component andsystem level testing to demonstrate product resilience from humanbody model (HBM), transmission line pulse (TLP), charged devicemodel (CDM), human metal model (HMM), cable discharge events (CDE),to system level IEC 61000-4-2 tests ESD on-chip design and process manufacturing practices andsolutions to improve ESD semiconductor chip solutions, alsopractical off-chip ESD protection and system level solutions toprovide more robust systems System level concerns in servers, laptops, disk drives, cellphones, digital cameras, hand held devices, automobiles, and spaceapplications Examples of ESD design for state-of-the-art technologies,including CMOS, BiCMOS, SOI, bipolar technology, high voltage CMOS(HVCMOS), RF CMOS, smart power, magnetic recording technology,micro-machines (MEMs) to nano-structures ESD Basics: From Semiconductor Manufacturing to ProductUse complements the author's series of books on ESDprotection. For those new to the field, it is an essentialreference and a useful insight into the

issues that confront moderntechnology as we enter the Nano-electronic Era.

Simulation Methods for ESD Protection DevelopmentElsevier

This useful book addresses electrothermal problems in modern VLSI systems. It discusses electrothermal phenomena and the fundamental building blocks that electrothermal simulation requires. The authors present three important applications of VLSI electrothermal analysis: temperature-dependent electromigration diagnosis, cell-level thermal placement, and temperature-driven power and timing analysis.

This book addresses the increasing demands from the industrial electronic engineers for reference materials on both theories and hands-on design skills for electrostatic discharge (ESD) protection designs, and the needs from college students to learn the same for their future career. Based on the author’s 25+ years of design and teaching experience, and research outcomes on the topic, this book is structured to cover all important aspects for on-chip ESD protection designs for integrated circuits (ICs), from theories to design skills to computer-aided design (CAD) methods, covering ESD phenomena, ESD failures, ESD test models, ESD protection devices, ESD protection circuits, ESD co-design methodology for high-performance mixed-signal ICs and broadband radio-frequency

(RF) ICs, and more.

This volume contains the proceedings of the 10th edition of the International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2004), held in Munich, Germany, on September 2-4, 2004. The conference program included 7 invited plenary lectures and 82 contributed papers for oral or poster presentation, which were carefully selected out of a total of 151 abstracts submitted from 14 countries around the world. Like the previous meetings, SISPAD 2004 provided a world-wide forum for the presentation and discussion of recent advances and developments in the theoretical description, physical modeling and numerical simulation and analysis of semiconductor fabrication processes, device operation and system performance. The variety of topics covered by the conference contributions reflects the physical effects and technological problems encountered in consequence of the progressively shrinking device dimensions and the ever-growing complexity in device technology.

This book addresses key aspects of analog integrated circuits and systems design related to system level electrostatic discharge (ESD) protection. It is an invaluable reference for anyone developing systems-on-chip (SoC) and systems-on-package (SoP), integrated with system-level ESD protection. The book focuses on both the design of

semiconductor integrated circuit (IC) components with embedded, on-chip system level protection and IC-system co-design. The readers will be enabled to bring the system level ESD protection solutions to the level of integrated circuits, thereby reducing or completely eliminating the need for additional, discrete components on the printed circuit board (PCB) and meeting system-level ESD requirements. The authors take a systematic approach, based on IC-system ESD protection co-design. A detailed description of the available IC-level ESD testing methods is provided, together with a discussion of the correlation between IC-level and system-level ESD testing methods. The IC-level ESD protection design is demonstrated with representative case studies which are analyzed with various numerical simulations and ESD testing. The overall methodology for IC-system ESD co-design is presented as a step-by-step procedure that involves both ESD testing and numerical simulations.

Provides new or expanded coverage on the latest techniques for microelectronic failure analysis. The CD-ROM includes the complete content of the book in fully searchable Adobe Acrobat format. Developed by the Electronic Device Failure Analysis Society (EDFAS) Publications Committee

Interest in latchup is being renewed with the evolution of complimentary metal-oxide semiconductor (CMOS) technology, metal-oxide-semiconductor field-effect transistor (MOSFET) scaling, and high-level system-on-chip (SOC) integration. Clear methodologies that grant protection from

latchup, with insight into the physics, technology and circuit issues involved, are in increasing demand. This book describes CMOS and BiCMOS semiconductor technology and their sensitivity to present day latchup phenomena, from basic over-voltage and over-current conditions, single event latchup (SEL) and cable discharge events (CDE), to latchup domino phenomena. It contains chapters focusing on bipolar physics, latchup theory, latchup and guard ring characterization structures, characterization testing, product level test systems, product level testing and experimental results. Discussions on state-of-the-art semiconductor processes, design layout, and circuit level and system level latchup solutions are also included, as well as: latchup semiconductor process solutions for both CMOS to BiCMOS, such as shallow trench, deep trench, retrograde wells, connecting implants, sub-collectors, heavily-doped buried layers, and buried grids – from single- to triple-well CMOS; practical latchup design methods, automated and bench-level latchup testing methods and techniques, latchup theory of logarithm resistance space, generalized alpha (a) space, beta (b) space, new latchup design methods– connecting the theoretical to the practical analysis, and; examples of latchup computer aided design (CAD) methodologies, from design rule checking (DRC) and logical-to-physical design, to new latchup CAD methodologies that address latchup for internal and external latchup on a local as well as global design level. Latchup acts as a companion text to the author's series of books on ESD (electrostatic discharge) protection, serving as an invaluable reference for the professional semiconductor chip and system-level ESD engineer. Semiconductor device, process and circuit designers, and quality, reliability and failure analysis engineers will find it informative on the issues that confront modern CMOS technology. Practitioners in the automotive and aerospace industries will also find it useful. In

addition, its academic treatment will appeal to both senior and graduate students with interests in semiconductor process, device physics, computer aided design and design integration.

Electrical overstress (EOS) and Electrostatic discharge (ESD) pose one of the most dominant threats to integrated circuits (ICs). These reliability concerns are becoming more serious with the downward scaling of device feature sizes. Modeling of Electrical Overstress in Integrated Circuits presents a comprehensive analysis of EOS/ESD-related failures in I/O protection devices in integrated circuits. The design of I/O protection circuits has been done in a hit-or-miss way due to the lack of systematic analysis tools and concrete design guidelines. In general, the development of on-chip protection structures is a lengthy expensive iterative process that involves tester design, fabrication, testing and redesign. When the technology is changed, the same process has to be repeated almost entirely. This can be attributed to the lack of efficient CAD tools capable of simulating the device behavior up to the onset of failure which is a 3-D electrothermal problem. For these reasons, it is important to develop and use an adequate measure of the EOS robustness of integrated circuits in order to address the on-chip EOS protection issue. Fundamental understanding of the physical phenomena leading to device failures under ESD/EOS events is needed for the development of device models and CAD tools that can efficiently describe the device behavior up to the onset of thermal failure. Modeling of Electrical Overstress in Integrated Circuits is for VLSI designers and reliability engineers, particularly those who are working on the development of EOS/ESD analysis tools. CAD engineers working on development of circuit level and device level electrothermal simulators will also benefit from the material covered. This book will also be of interest to researchers and

first and second year graduate students working in semiconductor devices and IC reliability fields.
An effective and cost efficient protection of electronic system against ESD stress pulses specified by IEC 61000-4-2 is paramount for any system design. This pioneering book presents the collective knowledge of system designers and system testing experts and state-of-the-art techniques for achieving efficient system-level ESD protection, with minimum impact on the system performance. All categories of system failures ranging from 'hard' to 'soft' types are considered to review simulation and tool applications that can be used. The principal focus of System Level ESD Co-Design is defining and establishing the importance of co-design efforts from both IC supplier and system builder perspectives. ESD designers often face challenges in meeting customers' system-level ESD requirements and, therefore, a clear understanding of the techniques presented here will facilitate effective simulation approaches leading to better solutions without compromising system performance. With contributions from Robert Ashton, Jeffrey Dunnihoo, Micheal Hopkins, Pratik Maheshwari, David Pomerenke, Wolfgang Reinprecht, and Matti Usumaki, readers benefit from hands-on experience and in-depth knowledge in topics ranging from ESD design and the physics of system ESD phenomena to tools and techniques to address soft failures and strategies to design ESD-robust systems that include mobile and automotive applications. The first dedicated resource to system-level ESD co-design, this is an essential reference for industry ESD designers, system builders, IC suppliers and customers and also Original Equipment Manufacturers (OEMs). Key features: Clarifies the concept of system level ESD protection. Introduces a co-design approach for ESD robust systems. Details soft and hard ESD fail mechanisms. Detailed protection strategies for both mobile and automotive

applications. Explains simulation tools and methodology for system level ESD co-design and overviews available test methods and standards. Highlights economic benefits of system ESD co-design.

This book brings together contributions from experts in the fields to describe the current status of important topics in solid-state circuit technologies. It consists of 20 chapters which are grouped under the following categories: general information, circuits and devices, materials, and characterization techniques. These chapters have been written by renowned experts in the respective fields making this book valuable to the integrated circuits and materials science communities. It is intended for a diverse readership including electrical engineers and material scientists in the industry and academic institutions. Readers will be able to familiarize themselves with the latest technologies in the various fields.

Predictive Simulation of Semiconductor Processing enables researchers and developers to extend the scaling range of semiconductor devices beyond the parameter range of empirical research. It requires a thorough understanding of the basic mechanisms employed in device fabrication, such as diffusion, ion implantation, epitaxy, defect formation and annealing, and contamination. This book presents an in-depth discussion of our current understanding of key processes and identifies areas that require further work in order to achieve the goal of a comprehensive, predictive process simulation tool.

Operational Amplifier Speed and Accuracy Improvement proposes a new methodology for the design of analog integrated circuits. The usefulness of this methodology is demonstrated through the design of an operational amplifier. This methodology consists of the following iterative steps: description of the circuit functionality at a high level of abstraction using signal flow graphs; equivalent

transformations and modifications of the graph to the form where all important parameters are controlled by dedicated feedback loops; and implementation of the structure using a library of elementary cells. Operational Amplifier Speed and Accuracy Improvement shows how to choose structures and design circuits which improve an operational amplifier's important parameters such as speed to power ratio, open loop gain, common-mode voltage rejection ratio, and power supply rejection ratio. The same approach is used to design clamps and limiting circuits which improve the performance of the amplifier outside of its linear operating region, such as slew rate enhancement, output short circuit current limitation, and input overload recovery.

Advanced level consolidation of the technology, physicsand design aspects of silicon-on-insulator (SOI)lubistors No comprehensive description of the physics and possibleapplications of the Lubistor can be found in a single source eventhough the Lubistor is already being used in SOI LSIs. The bookprovides, for the first time, a comprehensive understanding of thephysics of the Lubistor. The author argues that a clearunderstanding of the fundamental physics of the pn junction isessential to allowing scientists and engineers to propose newdevices. Since 2001 IBM has been applying the Lubistor tocommercial SOI LSIs (large scale integrated devices) used in PCsand game machines. It is a key device in that it provideselectrostatic protection to the LSIs. The book explains thedevice modeling for such applications, and covers the recent analogcircuit application of the voltage reference circuit. The author also reviews the physics and the modeling of idealand non-ideal pn junctions through reconsideration of theShockley's theory, offering readers an opportunity to studythe physics of pn junction. Pn-junction devices are alreadyapplied to the optical communication system as the light emitterand the receiver.

Alternatively, optical signal modulatorsare proposed for coupling the Si optical waveguide with thepn-junction injector. The book also explores the photoniccrystal physics and device applications of the Lubistor. Advanced level consolidation of the technology, physics anddesign aspects of silicon-on-insulator (SOI) lubistors Written by the inventor of the Lubistor, this volume describesthe technology for readers to understand the physics andapplications of the device First book devoted to the Lubistor transistor, presently beingutilized in electrostatic discharge (ESD) applications in SOItechnology, a growing market for semiconductor devices and advancedtechnologies Approaches the topic in a systematic manner, from physicaltheory, through to modelling, and finally circuit applications This is an advanced level book requiring knowledge of electricaland electronics engineering at graduate level. Contents includes: Concept of Ideal pn Junction/Proposalof Lateral, Unidirectional, Bipolar-Type Insulated-Gate Transistor(Lubistor)/ Noise Characteristics and Modeling of Lubistor/NegativeConductance Properties in Extremely Thin SOI Lubistors/ Two-Dimensionally Confined Injection Phenomena at LowTemperatures in Sub-10-nm-Thick SOI Lubistors/ Experimental Studyof Two-Dimensional Confinement Effects on Reverse-Biased CurrentCharacteristics of Ultra-Thin SOI Lubistors/ Gate-Controlled Bipolar Action in Ultra-thin Dynamic ThresholdSOI MOSFET/Sub-Circuit Models of SOI Lubistors for ElectrostaticDischarge Protection Circuit Design and Their Applications/A NewBasic Element for Neural Logic Functions and Functionality inCircuit Applications/Possible Implementation of SOI Lubistors intoConventional Logic Circuits/Potentiality of Electro-Optic ModulatorBased on SOI Waveguide/Principles of ParameterExtraction/Feasibility of Lubistor-Based Avalanche PhotoTransistor

This book introduces a new approach to model and predict substrate parasitic failures in integrated circuits with standard circuit design tools. The injection of majority and minority carriers in the substrate is a recurring problem in smart power ICs containing high voltage, high current switching devices besides sensitive control, protection and signal processing circuits. The injection of parasitic charges leads to the activation of substrate bipolar transistors. This book explores how these events can be evaluated for a wide range of circuit topologies. To this purpose, new generalized devices implemented in Verilog-A are used to model the substrate with standard circuit simulators. This approach was able to predict for the first time the activation of a latch-up in real circuits through post-layout SPICE simulation analysis. Discusses substrate modeling and circuit-level simulation of parasitic bipolar device coupling effects in integrated circuits; Includes circuit back-annotation of the parasitic lateral n-p-n and vertical p-n-p bipolar transistors in the substrate; Uses Spice for simulation and characterization of parasitic bipolar transistors, latch-up of the parasitic p-n-p-n structure, and electrostatic discharge (ESD) protection devices; Offers design guidelines to reduce couplings by adding specific protections.

The goal of putting `systems on a chip' has been a difficult challenge that is only recently being met. Since the world is `analog', putting systems on a chip requires putting analog interfaces on the same chip as digital processing functions. Since some processing functions are accomplished more efficiently in analog circuitry, chips with a large amount of analog and digital circuitry are being designed. Whether a small amount of analog circuitry is combined with varying amounts of digital circuitry or the other way around, the problem encountered in marrying analog and digital circuitry are the same but with different scope. Some of the most

prevalent problems are chip/package capacitive and inductive coupling, ringing on the RLC tuned circuits that form the chip/package power supply rails and off-chip drivers and receivers, coupling between circuits through the chip substrate bulk, and radiated emissions from the chip/package interconnects. To aggravate the problems of designers who have to deal with the complexity of mixed-signal coupling there is a lack of verification techniques to simulate the problem. In addition to considering RLC models for the various chip/package/board level parasitics, mixed-signal circuit designers must also model coupling through the common substrate when simulating ICs to obtain an accurate estimate of coupled noise in their designs. Unfortunately, accurate simulation of substrate coupling has only recently begun to receive attention, and techniques for the same are not widely known. Simulation Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits addresses two major issues of the mixed-signal coupling problem -- how to simulate it and how to overcome it. It identifies some of the problems that will be encountered, gives examples of actual hardware experiences, offers simulation techniques, and suggests possible solutions. Readers of this book should come away with a clear directive to simulate their design for interactions prior to building the design, versus a `build it and see' mentality.

* Examines the various methods available for circuit protection, including coverage of the newly developed ESD circuit protection schemes for VLSI circuits. * Provides guidance on the implementation of circuit protection measures. * Includes new sections on ESD design rules, layout approaches, package effects, and circuit concepts. * Reviews the new Charged Device Model (CDM) test method and evaluates design requirements necessary for circuit protection.

Electrostatic discharge (ESD) continues to impact semiconductor components and systems as technologies scale from micro- to nano-electronics. This book studies electrical overstress, ESD, and latchup from a whole-chip ESD design synthesis approach. It provides a clear insight into the integration of ESD protection networks from a generalist perspective, followed by examples in specific technologies, circuits, and chips. Uniquely both the semiconductor chip integration issues and floorplanning of ESD networks are covered from a ‘top-down' design approach. Look inside for extensive coverage on: integration of cores, power bussing, and signal pins in DRAM, SRAM, CMOS image processing chips, microprocessors, analog products, RF components and how the integration influences ESD design and integration architecturing of mixed voltage, mixed signal, to RF design for ESD analysis floorplanning for peripheral and core I/O designs, and the implications on ESD and latchup guard ring integration for both a ‘bottom-up' and ‘top-down' methodology addressing I/O guard rings, ESD guard rings, I/O to I/O, and I/O to core classification of ESD power clamps and ESD signal pin circuitry, and how to make the correct choice for a given semiconductor chip examples of ESD design for the state-of-the-art technologies discussed, including CMOS, BiCMOS, silicon on insulator (SOI), bipolar technology, high voltage CMOS (HVCMOS), RF CMOS, and smart power practical methods for the understanding of ESD circuit power distribution, ground rule development, internal bus distribution, current path analysis, quality metrics ESD: Design and Synthesis is a continuation of the author's series of books on ESD protection. It is an essential reference for: ESD, circuit, and semiconductor engineers; design synthesis team leaders; layout design, characterisation, floorplanning, test and reliability engineers; technicians; and groundrule and test site developers in the manufacturing and design of

semiconductor chips. It is also useful for graduate and undergraduate students in electrical engineering, semiconductor sciences, and manufacturing sciences, and on courses involving the design of ESD devices, chips and systems. This book offers a useful insight into the issues that confront modern technology as we enter the nano-electronic era.

This comprehensive and insightful book discusses ESD protection circuit design problems from an IC designer's perspective. On-Chip ESD Protection for Integrated Circuits: An IC Design Perspective provides both fundamental and advanced materials needed by a circuit designer for designing ESD protection circuits, including: Testing models and standards adopted by U.S. Department of Defense, EIA/JEDEC, ESD Association, Automotive Electronics Council, International Electrotechnical Commission, etc. ESD failure analysis, protection devices, and protection of sub-circuits Whole-chip ESD protection and ESD-to-circuit interactions Advanced low-parasitic compact ESD protection structures for RF and mixed-signal IC's Mixed-mode ESD simulation-design methodologies for design prediction ESD-to-circuit interactions, and more! Many real world ESD protection circuit design examples are provided. The book can be used as a reference book for working IC designers and as a textbook for students in the IC design field.

Les défaillances induites par les décharges électrostatiques (ESD) constituent un problème majeur de fiabilité et de robustesse des circuits intégrés et des systèmes électroniques. Dans certaines applications comme celles de l’automobile, ce pourcentage peut être proche de 20 %. Les problèmes de défaillance catastrophiques induits par des décharges électrostatiques n’ont commencé à être sérieusement pris en compte qu’avec l’avènement des technologies microélectroniques et la large diffusion de leurs

applications dans notre vie quotidienne. Cet ouvrage examine les diverses méthodologies de protection ESD et montre par le biais de cas concrets que la meilleure approche en termes de robustesse et de coût consiste à mettre en oeuvre une stratégie globale de protection ESD. Cette approche est déclinée du composant au système pour proposer des techniques d'investigation et des méthodologies de simulation prédictive associées, validées sur différents cas d'étude.

A practical and comprehensive reference that explores Electrostatic Discharge (ESD) in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems. Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection. Written by a noted expert on the topic, the text offers a topic-by-topic reference that includes illustrative figures, discussions, and drawings. The handbook covers a wide-range of topics including ESD in manufacturing (garments, wrist straps, and shoes); ESD Testing; ESD device physics; ESD semiconductor process effects; ESD failure mechanisms; ESD circuits in different technologies (CMOS, Bipolar, etc.); ESD circuit types (Pin, Power, Pin-to-Pin, etc.); and much more. In addition, the text includes a glossary, index, tables, illustrations, and a variety of case studies. Contains a well-organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications

Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians, operators, engineers, circuit designers, and failure analysis engineers, The ESD Handbook contains an accessible reference to ESD design and ESD systems.

"Written to address the needs of the ESD engineer in industry who is developing robust ESD concepts, it also gives deeper insight into devices operating at extreme current densities and temperatures and as such it should also be a valuable source of information for electrical engineering students and research scientists with a special interest in IC design and simulation techniques."--BOOK JACKET.

ESD Protection Device and Circuit Design for Advanced CMOS Technologies is intended for practicing engineers working in the areas of circuit design, VLSI reliability and testing domains. As the problems associated with ESD failures and yield losses become significant in the modern semiconductor industry, the demand for graduates with a basic knowledge of ESD is also increasing. Today, there is a significant demand to educate the circuits design and reliability teams on ESD issues. This book makes an attempt to address the ESD design and implementation in a systematic manner. A design procedure involving device simulators as well as circuit simulator is employed to optimize device and circuit parameters for optimal ESD as well as circuit performance. This methodology, described in ESD Protection Device and Circuit Design for Advanced CMOS Technologies has resulted in several successful

ESD circuit design with excellent silicon results and demonstrates its strengths.

The book all semiconductor device engineers must read to gain a practical feel for latchup-induced failure to produce lower-cost and higher-density chips. Transient-Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout. Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup, explaining the critical issues that have resurfaced for CMOS technologies. Once readers can gain an understanding of the standard practices for TLU, Ker and Hsu discuss the physical mechanism of TLU under a system-level ESD test, while introducing an efficient component-level TLU measurement setup. The authors then present experimental methodologies to extract safe and area-efficient compact layout rules for latchup prevention, including layout rules for I/O cells, internal circuits, and between I/O and internal circuits. The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0.18-micrometer 1.8V/3.3V silicided CMOS process. Presents real cases and solutions that occur in commercial CMOS IC chips Equips engineers with the skills to conserve chip layout area and decrease time-to-market Written by experts with real-world experience in circuit design and failure analysis Distilled from numerous courses taught by the authors in IC design houses worldwide The only book to introduce TLU under system-level ESD and EFT tests This book is

essential for practicing engineers involved in IC design, IC design management, system and application design, reliability, and failure analysis. Undergraduate and postgraduate students, specializing in CMOS circuit design and layout, will find this book to be a valuable introduction to real-world industry problems and a key reference during the course of their careers.

Failures caused by electrostatic discharges (ESD) constitute a major problem concerning the reliability and robustness of integrated circuits and electronic systems. This book summarizes the many diverse methodologies aimed at ESD protection and shows, through a number of concrete studies, that the best approach in terms of robustness and cost-effectiveness consists of implementing a global strategy of ESD protection. ESD Protection Methodologies begins by exploring the various normalized test techniques that are used to qualify ESD robustness as well as characterization and defect localization methods aimed at implementing corrective measures. Due to the increasing complexity of integrated circuits, it is important to be able to provide a simulation in which the implemented ESD protection strategy provides the desired protection, while not harming the performance levels of the circuit. Therefore, the main features and difficulties related to the different types of simulation, finite element, SPICE-type and behavioral, are then studied. To conclude, several case studies are presented which provide real-life examples of the approaches explained in the previous chapters and validate a number of the strategies from component to system level. Provides a global ESD protection approach

from component to system, including both the proposal of investigation techniques and predictive simulation methodologies Addresses circuit and system designers as well as failure analysis engineers Provides the description of specifically developed investigation techniques and the application of the proposed methodologies to real case studies

This book on electrostatic discharge phenomena is essentially a translation and update ofa Swedish edition from 1992. The book is intended for people working with electronic circuits and equipments, in application and development. All personnel should be aware of the ESD-hazards, especially those responsible for quality. ESD-prevention is a part of TQM (Total Quality Management). The book is also usable for courses on the subject. Background It was soon realised that the MOS-circuits (MOS=Metal Oxide Semiconductor), which appeared in the beginning of the 1960-ties were sensitive to electrostatic discharges. But a severe accident accelerated the search for materials that do not generate electric charges. In April 1964 three people were working inside a satellite at Cape Kennedy Space Center. They suddenly screamed "we are burning". They died. The satellite incapsulation was covered with untreated plastics to protect against dust. When the plastics was pulled off both this and the metal incapsulating got charged. A discharge from the metal ignited inflammable parts of the satellite. Eleven more people were injured and the cost of the accident amounted to about 55 billions USD.

Number 12 in the successful series of Analog Circuit

Design provides valuable information and excellent overviews of analogue circuit design, CAD and RF systems. The series is an ideal reference for those involved in analogue and mixed-signal design. Simulation Methods for ESD Protection Development looks at the integration of new techniques into a comprehensive development flow, which is now available due advances made in the field during the recent years. These findings allow for an early, stable ESD concept at a very early stage of the technology development, which is essential now development cycles have been reduced. The book also offers ways of increasing the optimization and control of the technology concerning performance, thus making the process more cost effective and increasingly efficient. This title provides a guide through the latest research and technology presenting the ESD protection development methodology. This is based on a combination of process, device and circuit stimulation, and addresses the optimization of the industry critical issue, reduced development cycles.Written to address the needs of the ESD engineer, this text is required reading by all industry practitioners and researchers and students within this field. The FIRST Extensive overview on the subject of ESD simulation Addresses the industry critical issue of reduced development cycles, and provides solutions Presents the latest research in the field with high practical relevance and its results

This Book and Simulation Software Bundle Project Dear Reader, this book project brings to you a unique study tool for ESD protection solutions used in analog-integrated circuit (IC) design. Quick-start learning is

combined with in-depth understanding for the whole spectrum of cro- disciplinary knowledge required to excel in the ESD ?eld. The chapters cover technical material from elementary semiconductor structure and device levels up to complex analog circuit design examples and case studies. The book project provides two different options for learning the material. The printed material can be studied as any regular technical textbook. At the same time, another option adds parallel exercise using the trial version of a complementary commercial simulation tool with prepared simulation examples. Combination of the textbook material with numerical simulation experience presents a unique opportunity to gain a level of expertise that is hard to achieve otherwise. The book is bundled with simpli?ed trial version of commercial mixed- TM mode simulation software from Angstrom Design Automation. The DECIMM (Device Circuit Mixed-Mode) simulator tool and complementary to the book s- ulation examples can be downloaded from www.analogesd.com. The simulation examples prepared by the authors support the speci?c examples discussed across the book chapters. A key idea behind this project is to provide an opportunity to not only study the book material but also gain a much deeper understanding of the subject by direct experience through practical simulation examples.

This thesis describes a novel distributed electrostatic charge distribution model and a new circuit-level simulation method to enable accurate full-chip CDM ESD protection circuit simulation, aiming to achieve CDM ESD protection design prediction and hence, first-Silicon

design success in developing CDM ESD protection solutions for advanced ICs. The new CDM ESD model and simulation techniques developed was verified in ICs implemented in a commercial 28nm CMOS technology.