Programmable Logic University Of California Berkeley

There is arguably no field in greater need of a comprehensive handbook than computer engineering. The unparalleled rate of technological advancement, the explosion of computer applications, and the now-in-progress migration to a wireless world have made it difficult for engineers to keep up with all the developments in specialties outside their own. References published only a few years ago are now sorely out of date. The Computer Engineering Handbook changes all of that. Under the leadership of Vojin Oklobdzija and a stellar editorial board, some of the industry's foremost experts have joined forces to create what promises to be the definitive resource for computer design and engineering. Instead of focusing on basic, introductory material, it forms a comprehensive, state-of-the-art review of the field's most recent achievements, outstanding issues, and future directions. The world of computer engineering is vast and evolving so rapidly that what is cutting-edge today may be obsolete in a few months. While exploring the new developments, trends, and future directions of the field, The Computer Engineering Handbook captures what is fundamental and of lasting value.
Module Generation Systems for Programmable Logic Arrays and Data PathsResearch ProjectStudies in Automatic Programming LogicNorth Holland
This book constitutes the refereed proceedings of the 8th International Workshop on Field-Programmable Logics and Applications, FPL '98, held in Tallinn, Estonia, in August/September 1998. The 39 revised full papers presented were carefully selected for inclusion in the book

from a total of 86 submissions. Also included are 30 refereed high-quality posters. The papers are organized in topical sections on design methods, general aspects, prototyping and simulation, development methods, accelerators, system architectures, hardware/software codesign, system development, algorithms on FPGAs, and applications.

Low-Energy FPGAs: Architecture and Design is a primary resource for both researchers and practicing engineers in the field of digital circuit design. The book addresses the energy consumption of Field-Programmable Gate Arrays (FPGAs). FPGAs are becoming popular as embedded components in computing platforms. The programmability of the FPGA can be used to customize implementations of functions on an application basis. This leads to performance gains, and enables reuse of expensive silicon. Chapter 1 provides an overview of digital circuit design and FPGAs. Chapter 2 looks at the implication of deep-submicron technology onFPGA power dissipation. Chapter 3 describes the exploration environment to guide and evaluate design decisions. Chapter 4 discusses the architectural optimization process to evaluate the trade-offs between the flexibility of the architecture, and the effect on the performance metrics. Chapter 5 reviews different circuit techniques to reduce the performance overhead of some of the dominant components. Chapter 6 shows methods to configure FPGAs to minimize the programming overhead. Chapter 7 addresses the physical realization of some of the critical components and the final implementation of a specific low-energy FPGA. Chapter 8 compares the prototype array to an equivalent commercial architecture.

VLSI systems are becoming very complex and difficult to test. Traditional stuck-at fault problems may be inadequate to model possible manufacturing defects in the integrated ciruit. Hierarchial models are needed that are easy to use at the transistor and functional levels.

Stuck-open faults present severe testing problems in CMOS circuits, to overcome testing problems testable designs are utilized. Bridging faults are important due to the shrinking geometry of ICs. BIST PLA schemes have common features-controllability and observability - which are enhanced through additional logic and test points. Certain circuit topologies are more easily testable than others. The amount of reconvergent fan-out is a critical factor in determining realistic measures for determining test generation difficulty. Test implementation is usually left until after the VLSI data path has been synthesized into a structural description. This leads to investigation methodologies for performing design synthesis with test incorporation. These topics and more are discussed.

This book presents the original concepts and modern techniques for specification, synthesis, optimisation and implementation of parallel logical control devices. It deals with essential problems of reconfigurable control systems like dependability, modularity and portability. Reconfigurable systems require a wider variety of design and verification options than the application-specific integrated circuits. The book presents a comprehensive selection of possible design techniques. The diversity of the modelling approaches covers Petri nets, state machines and activity diagrams. The preferences of the presented optimization and synthesis methods are not limited to increasing of the efficiency of resource use. One of the biggest advantages of the presented methods is the platform independence, the FPGA devices and single board

computers are some of the examples of possible platforms. These issues and problems are illustrated with practical cases of complete control systems. If you expect a new look at the reconfigurable systems designing process or need ideas for improving the quality of the project, this book is a good choice.g process or need ideas for improving the quality of the project, this book is a good choice. Issues in Technology Theory, Research, and Application: 2011 Edition is a ScholarlyEditions™ eBook that delivers timely, authoritative, and comprehensive information about Technology Theory, Research, and Application. The editors have built Issues in Technology Theory, Research, and Application: 2011 Edition on the vast information databases of ScholarlyNews.™ You can expect the information about Technology Theory, Research, and Application in this eBook to be deeper than what you can access anywhere else, as well as consistently reliable, authoritative, informed, and relevant. The content of Issues in Technology Theory, Research, and Application: 2011 Edition has been produced by the world's leading scientists, engineers, analysts, research institutions, and companies. All of the content is from peer-reviewed sources, and all of it is written, assembled, and edited by the editors at ScholarlyEditions™ and available exclusively from us. You now have a source you can cite with authority, confidence, and credibility. More information is available at

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For the editors of this book, as well as for many other researchers in the area of fault-tolerant computing, Dr. William Caswell Carter is one of the key figures in the formation and development of this important field. We felt that the IFIP Working Group 10.4 at Baden, Austria, in June 1986, which coincided with an important step in Bill's career, was an appropriate occasion to honor Bill's contributions and achievements by organizing a one day "Symposium on the Evolution of Fault-Tolerant Computing" in the honor of William C. Carter. The Symposium, held on June 30, 1986, brought together a group of eminent scientists from all over the world to discuss the evolu tion, the state of the art, and the future perspectives of the field of fault-tolerant computing. Historic developments in academia and industry were presented by individuals who themselves have actively been involved in bringing them about. The Symposium proved to be a unique historic event and these Proceedings, which contain the final versions of the papers presented at Baden, are an authentic reference document.

Topics covered: Theoretical Foundations. Higher-Order Logics. Non-Monotonic Reasoning. Programming Methodology. Programming Environments. Extensions to Logic Programming. Constraint Satisfaction. Meta-Programming. Language

Design and Constructs. Implementation of Logic Programming Languages. Compilation Techniques. Architectures. Parallelism. Reasoning about Programs. Deductive Databases. Applications. 13-16 June 1995, Tokyo, Japan ICLP, which is sponsored by the Association for Logic Programming, is one of two major annual international conferences reporting recent research results in logic programming. Logic programming originates from the discovery that a subset of predicate logic could be given a procedural interpretation which was first embodied in the programming language, Prolog. The unique features of logic programming make it appealing for numerous applications in artificial intelligence, computer-aided design and verification, databases, and operations research, and for exploring parallel and concurrent computing. The last two decades have witnessed substantial developments in this field from its foundation to implementation, applications, and the exploration of new language designs. Topics covered: Theoretical Foundations. Higher-Order Logics. Non-Monotonic Reasoning. Programming Methodology. Programming Environments. Extensions to Logic Programming. Constraint Satisfaction. Meta-Programming. Language Design and Constructs. Implementation of Logic Programming Languages. Compilation Techniques. Architectures. Parallelism. Reasoning about Programs. Deductive Databases. Applications. Logic Programming series, Research

Reports and Notes

Programmable Logic Devices (PLDs) have become the key implementation medium for the vast majority of digital circuits designed today. While the highest-volume devices are still built with full-fabrication rather than field programmability, the trend towards ever fewer ASICs and more FPGAs is clear. This makes the field of PLD architecture ever more important, as there is stronger demand for faster, smaller, cheaper and lower-power programmable logic. PLDs are 90% routing and 10% logic. This book focuses on that 90% that is the programmable routing: the manner in which the programmable wires are connected and the circuit design of the programmable switches themselves. Anyone seeking to understand the design of an FPGA needs to become lit erate in the complexities of programmable routing architecture. This book builds on the state-of-the-art of programmable interconnect by providing new methods of investigating and measuring interconnect structures, as well as new programmable switch basic circuits. The early portion of this book provides an excellent survey of interconnec tion structures and circuits as they exist today. Lemieux and Lewis then provide a new way to design sparse crossbars as they are used in PLDs, and show that the method works with an empirical validation. This is one of a few routing architecture works that employ analytical methods to deal with the routing archi

tecture design. The analysis permits interesting insights not typically possible with the standard empirical approach.

This book is the proceedings volume of the 10th International Conference on Field Programmable Logic and its Applications (FPL), held August 27 30, 2000 in Villach, Austria, which covered areas like reconfigurable logic (RL), reconfigurable computing (RC), and its applications, and all other aspects. Its subtitle "The Roadmap to Reconfigurable Computing" reminds us, that we are currently witnessing the runaway of a breakthrough. The annual FPL series is the eldest international conference in the world covering configware and all its aspects. It was founded 1991 at Oxford University (UK) and is 2 years older than its two most important competitors usually taking place at Monterey and Napa. FPL has been held at Oxford, Vienna, Prague, Darmstadt, London, Tallinn, and Glasgow (also see: http://www. fpl. uni kl. de/FPL/). The New Case for Reconfigurable Platforms: Converging Media. Indicated by palmtops, smart mobile phones, many other portables, and consumer electronics, media such as voice, sound, video, TV, wireless, cable, telephone, and Internet continue to converge. This creates new opportunities and even necessities for reconfigurable platform usage. The new converged media require high volume, flexible, multi purpose, multi standard, low power products adaptable to support evolving standards, emerging new standards, field upgrades, bug fixes, and, to meet the needs of a growing number of different kinds of services offered to zillions of individual subscribers preferring different media mixes.

This book constitutes the refereed proceedings of the 4th International Conference on Tools and Algorithms for the Construction and Analysis of Systems, TACAS'98, held in conjunction

with ETAPS in Lisbon, Portugal, in March/April 1998. The 28 revised full papers presented together with an invited talk were selected from a total of 78 submissions. The volume is devoted to conceptual foundations, development, and applications of tools and algorithms for the specification, verification, analysis, and construction of software and hardware systems. The papers are organized in sections on model checking, design and architecture, various applications, fielded applications, verification of real-time systems, mixed analysis techniques, and case studies and experience.

This book constitutes the refereed proceedings of the 13th International Conference on Field-Programmable Logic and Applications, FPL 2003, held in Lisbon, Portugal in September 2003. The 90 revised full papers and 56 revised poster papers presented were carefully reviewed and selected from 216 submissions. The papers are organized in topical sections on technologies and trends, communications applications, high level design tools, reconfigurable architecture, cryptographic applications, multi-context FPGAs, low-power issues, run-time reconfiguration, compilation tools, asynchronous techniques, bio-related applications, codesign, reconfigurable fabrics, image processing applications, SAT techniques, application-specific architectures, DSP applications, dynamic reconfiguration, SoC architectures, emulation, cache design, arithmetic, bio-inspired design, SoC design, cellular applications, fault analysis, and network applications.

Illustrates how intelligent systems can be applied to the verification, debugging, and synthesis of computer programs.

Featuring hundreds of illustrations and references, this volume in the third edition of the Circuits and Filters Handbook, provides the latest information on analog and VLSI circuits,

omitting extensive theory and proofs in favor of numerous examples throughout each chapter. The first part of the text focuses on analog integrated circuits, presenting up-to-date knowledge on monolithic device models, analog circuit cells, high performance analog circuits, RF communication circuits, and PLL circuits. In the second half of the book, well-known contributors offer the latest findings on VLSI circuits, including digital systems, data converters, and systolic arrays.

A bestseller in its first edition, The Circuits and Filters Handbook has been thoroughly updated to provide the most current, most comprehensive information available in both the classical and emerging fields of circuits and filters, both analog and digital. This edition contains 29 new chapters, with significant additions in the areas of computer-

This monograph provides an intensive course for graduate students in computer science, as well as others interested in extensions of logic programming, on the theoretical foundations of disjunctive logic programming. Disjunctive logic programming permits the description of indefinite or incomplete information through a disjunction of atoms in the head of a clause. The authors describe model theoretic semantics, proof theoretic semantics, and fix point semantics for disjunctive and normal disjunctive programs (a normal disjunctive program permits negated atoms in the body of a clause) and present theories of negation.

They conclude with selected applications to knowledge databases. Jorge Lobo is Assistant Professor in Computer Science at the University of Illinois, Chicago Circle. Jack Minker is Professor in the Department of Computer Science and Institute for Advanced Computer Studies at the University of Maryland. Arcot Rajasekar is Assistant Professor in the Computer Science Department at the University of Kentucky. Contents: Introduction and Background. Definitions and Terminology. Declarative Semantics. Proof Theory. Negation. Weak Negation. Normal Logic Programs. Procedural Semantics: Normal Programs. Disjunctive Databases. Applications.

This book focuses on foundry-based process technology that enables the fabrication of 3-D ICs. The core of the book discusses the technology platform for pre-packaging wafer lever 3-D ICs. However, this book does not include a detailed discussion of 3-D ICs design and 3-D packaging. This is an edited book based on chapters contributed by various experts in the field of wafer-level 3-D ICs process technology. They are from academia, research labs and industry.

This book contains the papers presented at the 14th International Conference on Field Programmable Logic and Applications (FPL) held during August 30th-September 1st 2004. The conference was hosted by the Interuniversity Micro-Electronics Center (IMEC) in Leuven, Belgium. The FPL series of conferences

was founded in 1991 at Oxford University (UK), and has been held annually since: in Oxford (3 times), Vienna, Prague, Darmstadt, London, Tallinn, Glasgow, Villach, Belfast, Montpellier and Lisbon. It is the largest and oldest conference in reconfigurable computing and brings together academic researchers, industry experts, users and newcomers in an informal, welcoming atmosphere that encourages productive exchange of ideas and knowledge between the delegates. The fast and exciting advances in field programmable logic are increasing steadily with more and more application potential and need. New ground has been broken in architectures, design techniques, (partial) run-time reconfiguration and applications of field programmable devices in several different areas. Many of these recent innovations are reported in this volume. The size of the FPL conferences has grown significantly over the years. FPL in 2003 saw 216 papers submitted. The interest and support for FPL in the programmable logic community continued this year with 285 scientific papers submitted, demonstrating a 32% increase when compared to the year before. The technical program was assembled from 78 selected regular papers, 45 additional short papers and 29 posters, resulting in this volume of proceedings. The program also included three invited plenary keynote presentations from Xilinx, Gilder Technology Report and Altera, and three embedded tutorials from

Xilinx, the Universit ? at Karlsruhe (TH) and the University of Oslo.
This volume contains the proceedings of the 4th International Workshop on Field-Programmable Logic and Applications (FPL '94), held in Prague, Czech Republic in September 1994. The growing importance of field-programmable devices is substantiated by the remarkably high number of 116 submissions for FPL '94; from them, the revised versions of 40 full papers and 24 high-quality poster presentations were accepted for inclusion in this volume. Among the topics treated are: testing, layout, synthesis tools, compilation research and CAD, trade-offs and experience, innovations and smart applications, FPGA-based computer architectures, high-level design, prototyping and ASIC emulators, commercial devices, new tools, CCMs and HW/SW co-design, modelers, educational experience, and novel architectures.
This volume constitutes the proceedings of the Fifth International Workshop on Field-Programmable Logic and Its Applications, FPL '95, held in Oxford, UK in August/September 1995. The volume presents 46 full revised papers carefully selected by the program committee from a large number and wide range of submissions. The papers document the progress achieved since the predecessor conference (see LNCS 849). They are organized in sections on architectures, platforms, tools, arithmetic and signal processing, embedded systems and other applications, and reconfigurable

design and models.

This book contains the papers presented at the 9th International Workshop on Field ProgrammableLogic and Applications (FPL'99), hosted by the University of Strathclyde in Glasgow, Scotland, August 30 – September 1, 1999. FPL'99 is the ninth in the series of annual FPL workshops. The FPL'99 programme committee has been fortunate to have received a large number of high-quality papers addressing a wide range of topics. From these, 33 papers have been selected for presentation at the workshop and a further 32 papers have been accepted for the poster sessions. A total of 65 papers from 20 countries are included in this volume. FPL is a subject area that attracts researchers from both electronic engine- ing and computer science. Whether we are engaged in research into soft ha- ware or hard software seems to be primarily a question of perspective. What is unquestionable is that the interaction of groups of researchers from di?erent backgrounds results in stimulating and productive research. As we prepare for the new millennium, the premier European forum for - searchers in ?eld programmable logic remains the FPL workshop. Next year the FPL series of workshopswill celebrate its tenth anniversary.The contribution of so many overseas researchers has been a particularly attractive feature of these events, giving them a truly international perspective, while the informal and convivial atmosphere that pervades the workshops have been their hallmark. We look forward to preserving these features in the future while continuing to expand the size and quality of the events.

Short turnaround has become critical in the design of electronic systems. Software-programmable components such as microprocessors and digital signal processors have been used extensively in such systems since they allow rapid design revisions. However, the inherent performance limitations of software-programmable systems mean that they are inadequate for high-performance designs. Designers thus turned to gate arrays as a solution. User-programmable gate arrays (field-programmable gate arrays, FPGAs) have recently emerged and are changing the way electronic systems are designed and implemented. The growing complexity of the logic circuits that can be packed onto an FPGA chip means that it has become important to have automatic synthesis tools that implement logic functions on these architectures. Logic Synthesis for Field-Programmable Gate Arrays describes logic synthesis for both look-up table (LUT) and multiplexor-based architectures, with a balanced presentation of existing techniques together with algorithms and the system developed by the authors. Audience: A useful reference for VLSI designers, developers of computer-aided design tools, and anyone involved in or with FPGAs.