Essentials Of Electronic Testing For Digital Memory And Mixed Signal Vlsi Circuits Frontiers In Electronic Testing

Embedded Processor-Based Self-Test is a guide to self-testing strategies for embedded processors. Embedded processors are regularly used today in most System-on-Chips (SoCs). Testing of microprocessors and embedded processors has always been a challenge because most traditional testing techniques fail when applied to them. This is due to the complex sequential structure of processor architectures, which consists of high performance datapath units and sophisticated control logic for performance optimization. Structured Design-for-Testability (DfT) and hardware-based self-testing techniques, which usually have a non-trivial impact on a circuit's performance, size and power, can not be applied without serious consideration and careful incorporation into the processor design. Embedded Processor-Based Self-Test shows how the powerful embedded functionality that processors offer can be utilized as a self-testing resource. Through a discussion of different strategies the book emphasizes on the emerging area of Software-Based Self-Testing (SBST). SBST is based on the idea of execution of embedded software programs to perform self-testing of the processor itself and its surrounding blocks in the SoC. SBST is a low-cost strategy in terms of overhead (area, speed, power), development effort and test application cost, as it is applied using low-cost, low-speed test equipment. Embedded Processor-Based Self-Test can be used by designers, DfT engineers, test practitioners, researchers and students working on digital testing, and in particular processor and SoC test. This book sets the framework for comparisons among different SBST methodologies by discussing key requirements. It presents successful applications of SBST to a number of embedded processors of different complexities and instruction set architectures.

This book provides an introduction to the cost modeling for electronic systems that is suitable for advanced undergraduate and graduate students in electrical, mechanical and industrial engineering, and professionals involved with electronics technology development and management. This book melds elements of traditional engineering economics with manufacturing process and life-cycle cost management concepts to form a practical foundation for predicting the cost of electronic products and systems. Various manufacturing cost analysis methods are addressed including: process-flow, parametric, cost of ownership, and activity based costing. The effects of learning curves, data uncertainty, test and rework processes, and defects are considered. Aspects of system sustainment and life-cycle cost modeling including reliability (warranty, burn-in), maintenance (sparing and availability), and obsolescence are treated. Finally, total cost of ownership of systems, return on investment, cost-benefit analysis, and real options analysis are addressed.

This book constitutes the refereed proceedings of the 16th International Symposium on VSLI Design and Test, VDAT 2012, held in Shibpur, India, in July 2012. The 30 revised regular papers presented together with 10 short papers and 13 poster sessions were carefully selected from 135 submissions. The papers are organized in topical sections on VLSI design, design and modeling of digital circuits and systems, testing and verification, design for testability, testing memories and regular logic arrays, embedded systems: hardware/software co-design and verification, emerging technology: nanoscale computing and nanotechnology.

This pioneering text explains how to synthesize digital diagnostic sequences for wire interconnects using boundary-scan, and how to assess the quality of those sequences. It takes a new approach, carefully modelling circuit and interconnect faults, and applying graph techniques to solve problems.

This book presents the research challenges that are due to the introduction of the 3rd dimension in chips for researchers and covers the whole architectural design approach for 3D-SoCs. Nowadays the 3D-Integration technologies, 3D-Design techniques, and 3D-Architectures are emerging as interesting, truly hot, broad topics. The present book gathers the recent advances in the whole domain by renowned experts in the field to build a comprehensive and consistent book around the hot topics of three-dimensional architectures and micro-architectures. This book includes contributions from high level international teams working in this field.

What the experts have to say about Model-Based Testing for Embedded Systems: "This book is exactly what is needed at the exact right time in this fast-growing area. From its beginnings over 10 years ago of deriving tests from UML statecharts, model-based testing has matured into a topic with both breadth and depth. Testing embedded systems is a natural application of MBT, and this book hits the nail exactly on the head. Numerous topics are presented clearly, thoroughly, and concisely in this cutting-edge book. The authors are world-class leading experts in this area and teach us well-used and validated techniques, along with new ideas for solving hard problems. "It is rare that a book can take recent research advances and present them in a form ready for practical use, but this book accomplishes that and more. I am anxious to recommend this in my consulting and to teach a new class to my students." —Dr. Jeff Offutt, professor of software engineering, George Mason University, Fairfax, Virginia, USA "This handbook is the best resource I am aware of on the automated testing of embedded systems. It is thorough, comprehensive, and authoritative. It covers all important technical and scientific aspects but also provides highly interesting insights into the state of practice of model-based testing for embedded systems." —Dr. Lionel C. Briand, IEEE Fellow, Simula Research Laboratory, Lysaker, Norway, and professor at the University of Oslo, Norway "As model-based testing is entering the mainstream, such a comprehensive and intelligible book is a must-read for anyone looking for more information about improved testing methods for embedded systems. Illustrated with numerous aspects of these techniques from many contributors, it gives a clear picture of what the state of the art is today." —Dr. Bruno Legeard, CTO of Smartesting, professor of Software Engineering at the University of Franche-Comté, Besançon, France, and co-author of Practical Model-Based Testing

This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product, drive down test cost, improve product quality and yield, and speed up time-to-market and time-to-volume. Most up-to-date coverage of design for testability. Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books. Numerous, practical examples in each chapter illustrating basic VLSI test principles and DFT architectures.

As the number of processor cores and IP blocks integrated on a single chip is steadily growing, a systematic approach to design the communication infrastructure becomes necessary. Different variants of packed switched on-chip networks have been proposed by several groups during the past two years. This book summarizes the state of the art of these efforts and discusses the major issues from the physical integration to architecture to operating systems and application interfaces. It also provides a guideline and vision about the direction this field is moving to. Moreover, the book outlines the consequences of adopting design platforms based on packet switched network. The consequences may in fact be far reaching because many of the topics of distributed systems, distributed real-time systems, fault tolerant systems, parallel computer architecture, parallel programming as well as traditional system-on-chip issues will appear relevant but within the constraints of a single chip VLSI implementation.

This book will introduce new techniques for detecting and diagnosing small-delay defects in integrated circuits. Although this sort of timing defect is commonly

found in integrated circuits manufactured with nanometer technology, this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small-delay defects, including important parameters such as process variations, crosstalk, and power supply noise.

In a modern technological society, electronic engineering and design innovations are both academic and practical engineering fields that involve systematic technological materialization through scientific principles and engineering designs. Engineers and designers must work together with a variety of other professionals in their quest to find systems solutions to complex problems. Rapid advances in science and technology have broadened the horizons of engineering while simultaneously creating a multitude of challenging problems in every aspect of modern life. Current research is interdisciplinary in nature, reflecting a combination of concepts and methods that often span several areas of mechanics, mathematics, electrical engineering, control engineering, and other scientific disciplines. In addition, the 2nd IEEE International Conference on Knowledge Innovation and Invention 2019 (IEEE ICKII 2019) was held in Seoul, South Korea, on 12–15 July, 2019. This book, “Intelligent Electronic Devices”, includes 13 excellent papers form 260 papers presented in this conference about intelligent electronic devices. The main goals of this book were to encourage scientists to publish their experimental and theoretical results in as much detail as possible and to provide new scientific knowledge relevant to the topics of electronics.

Using the book and the software provided with it, the reader can build his/her own tester arrangement to investigate key aspects of analog-, digital- and mixed system circuits Plan of attack based on traditional testing, circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests Worked examples based on theoretical bookwork, practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively

This book describes efficient techniques for production testing as well as for periodic maintenance testing (specifically in terms of multi-cell faults) in modern semiconductor memory. The author discusses background selection and address reordering algorithms in multi-run transparent march testing processes. Formal methods for multi-run test generation and many solutions to increase their efficiency are described in detail. All methods presented ideas are verified by both analytical investigations and numerical simulations. Provides the first book related exclusively to the problem of multi-cell fault detection by multi-run tests in memory testing process; Presents practical algorithms for design and implementation of efficient multi-run tests; Demonstrates methods verified by analytical and experimental investigations.

This book is about digital system testing and testable design. The concepts of testing and testability are treated together with digital design practices and methodologies. The book uses Verilog models and testbenches for implementing

and explaining fault simulation and test generation algorithms. Extensive use of Verilog and Verilog PLI for test applications is what distinguishes this book from other test and testability books. Verilog eliminates ambiguities in test algorithms and BIST and DFT hardware architectures, and it clearly describes the architecture of the testability hardware and its test sessions. Describing many of the on-chip decompression algorithms in Verilog helps to evaluate these algorithms in terms of hardware overhead and timing, and thus feasibility of using them for System-on-Chip designs. Extensive use of testbenches and testbench development techniques is another unique feature of this book. Using PLI in developing testbenches and virtual testers provides a powerful programming tool, interfaced with hardware described in Verilog. This mixed hardware/software environment facilitates description of complex test programs and test strategies. Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance-capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost. This book is a comprehensive guide to new VLSI Testing and Design-for-Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly System-on-Chip Test architectures, for test debug and diagnosis of digital, memory, and analog/mixed-signal designs. Emphasizes VLSI Test principles and Design for Testability architectures, with numerous illustrations/examples. Most up-to-date coverage available, including Fault Tolerance, Low-Power Testing, Defect and Error Tolerance, Network-on-Chip (NOC) Testing, Software-Based Self-Testing, FPGA Testing, MEMS Testing, and System-In-Package (SIP) Testing, which are not yet available in any testing book. Covers the entire spectrum of VLSI testing and DFT architectures, from digital and analog, to memory circuits, and fault diagnosis and self-repair from digital to memory circuits. Discusses future nanotechnology test trends and challenges facing the nanometer design era; promising nanotechnology test techniques, including Quantum-Dots, Cellular Automata, Carbon-Nanotubes, and Hybrid Semiconductor/Nanowire/Molecular Computing. Practical problems at the end of each chapter for students.

This book provides broad and comprehensive coverage of the entire EDA flow. EDA/VLSI practitioners and researchers in need of fluency in an "adjacent" field will find this an invaluable reference to the basic EDA concepts, principles, data structures, algorithms, and architectures for the design, verification, and test of VLSI circuits. Anyone who needs to learn the concepts, principles, data structures, algorithms, and architectures of the EDA flow will benefit from this book. Covers complete spectrum of the EDA flow, from ESL design modeling to logic/test synthesis, verification, physical design, and test - helps EDA newcomers to get "up-and-running" quickly Includes comprehensive coverage of EDA concepts, principles, data structures, algorithms, and architectures - helps

all readers improve their VLSI design competence Contains latest advancements not yet available in other books, including Test compression, ESL design modeling, large-scale floorplanning, placement, routing, synthesis of clock and power/ground networks - helps readers to design/develop testable chips or products Includes industry best-practices wherever appropriate in most chapters - helps readers avoid costly mistakes

Testing Static Random Access Memories covers testing of one of the important semiconductor memories types; it addresses testing of static random access memories (SRAMs), both single-port and multi-port. It contributes to the technical acknowledge needed by those involved in memory testing, engineers and researchers. The book begins with outlining the most popular SRAMs architectures. Then, the description of realistic fault models, based on defect injection and SPICE simulation, are introduced. Thereafter, high quality and low cost test patterns, as well as test strategies for single-port, two-port and any p-port SRAMs are presented, together with some preliminary test results showing the importance of the new tests in reducing DPM level. The impact of the port restrictions (e.g., read-only ports) on the fault models, tests, and test strategies is also discussed. Features: -Fault primitive based analysis of memory faults, -A complete framework of and classification memory faults, -A systematic way to develop optimal and high quality memory test algorithms, -A systematic way to develop test patterns for any multi-port SRAM, -Challenges and trends in embedded memory testing.

This book reviews fault-tolerance techniques for SRAM-based Field Programmable Gate Arrays (FPGAs), outlining many methods for designing fault tolerance systems. Some of these are based on new fault-tolerant architecture, and others on protecting the high-level hardware description before synthesis in the FPGA. The text helps the reader choose the best techniques project-by-project, and to compare fault tolerant techniques for programmable logic applications.

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"This book covers aspects of system design and efficient modelling, and also introduces various fault models and fault mechanisms associated with digital circuits integrated into System on Chip (SoC), Multi-Processor System-on Chip (MPSoC) or Network on Chip (NoC)"--

Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits (ICs). However, the increased complexity and nanometer-size features of modern ICs make them susceptible to manufacturing defects, as well as performance and quality issues. Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens/bridges, and design-for-manufacturing (DfM)-related rule violations. The book also addresses testing for small-delay defects (SDDs), which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing, including basic concepts and introductory material Describes algorithmic solutions incorporated in

commercial tools from Mentor Graphics Reviews SDD testing based on "alternative methods" that explores new metrics, top-off ATPG, and circuit topology-based solutions Highlights the advantages and disadvantages of a diverse set of metrics, and identifies scope for improvement Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions.

This book introduces readers to various threats faced during design and fabrication by today's integrated circuits (ICs) and systems. The authors discuss key issues, including illegal manufacturing of ICs or "IC Overproduction," insertion of malicious circuits, referred as "Hardware Trojans", which cause in-field chip/system malfunction, and reverse engineering and piracy of hardware intellectual property (IP). The authors provide a timely discussion of these threats, along with techniques for IC protection based on hardware obfuscation, which makes reverse-engineering an IC design infeasible for adversaries and untrusted parties with any reasonable amount of resources. This exhaustive study includes a review of the hardware obfuscation methods developed at each level of abstraction (RTL, gate, and layout) for conventional IC manufacturing, new forms of obfuscation for emerging integration strategies (split manufacturing, 2.5D ICs, and 3D ICs), and on-chip infrastructure needed for secure exchange of obfuscation keys- arguably the most critical element of hardware obfuscation.

System-on-a-Chip (SOC) integrated circuits composed of embedded cores are now commonplace. Nevertheless, there remain several roadblocks to rapid and efficient system integration. Test development is seen as a major bottleneck in SOC design and manufacturing capabilities. Testing SOCs is especially challenging in the absence of standardized test structures, test automation tools, and test protocols. In addition, long interconnects, high density, and high-speed designs lead to new types of faults involving crosstalk and signal integrity. SOC (System-on-a-Chip) Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing. SOC (System-on-a-Chip) Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing.

The modern electronic testing has a forty year history. Test professionals hold some fairly large conferences and numerous workshops, have a journal, and there are over one hundred books on testing. Still, a full course on testing is offered only at a few universities, mostly by professors who have a research interest in this area. Apparently, most professors would not have taken a course on electronic testing when they were students. Other than the computer engineering curriculum being too crowded, the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook. For VLSI the foundation was provided by semiconductor device techn- ogy, circuit design, and electronic testing. In a computer engineering curriculum, therefore, it is necessary that foundations should be taught before applications. The field of VLSI has expanded to systems-on-a-chip, which include digital, memory, and mixed-signalsubsystems. To our knowledge this is the first textbook to cover all three types of electronic circuits. We have written this textbook for an undergraduate "foundations"

course on electronic testing. Obviously, it is too voluminous for a one-semester course and a teacher will have to select from the topics. We did not restrict such freedom because the selection may depend upon the individual expertise and interests. Besides, there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course. With equal tenacity, we address the needs of three other groups of readers.

Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI CircuitsSpringer Science & Business Media

This book provides an overview of automatic test pattern generation (ATPG) and introduces novel techniques to complement classical ATPG, based on Boolean Satisfiability (SAT). A fast and highly fault efficient SAT-based ATPG framework is presented which is also able to generate high-quality delay tests such as robust path delay tests, as well as tests with long propagation paths to detect small delay defects. The aim of the techniques and methodologies presented in this book is to improve SAT-based ATPG, in order to make it applicable in industrial practice. Readers will learn to improve the performance and robustness of the overall test generation process, so that the ATPG algorithm reliably will generate test patterns for most targeted faults in acceptable run time to meet the high fault coverage demands of industry. The techniques and improvements presented in this book provide the following advantages: Provides a comprehensive introduction to test generation and Boolean Satisfiability (SAT); Describes a highly fault efficient SAT-based ATPG framework; Introduces circuit-oriented SAT solving techniques, which make use of structural information and are able to accelerate the search process significantly; Provides SAT formulations for the prevalent delay faults models, in addition to the classical stuck-at fault model; Includes an industrial perspective on the state-of-the-art in the testing, along with SAT; two topics typically distinguished from each other.

Wafer-level testing refers to a critical process of subjecting integrated circuits and semiconductor devices to electrical testing while they are still in wafer form. Burn-in is a temperature/bias reliability stress test used in detecting and screening out potential early life device failures. This hands-on resource provides a comprehensive analysis of these methods, showing how wafer-level testing during burn-in (WLTBI) helps lower product cost in semiconductor manufacturing. Engineers learn how to implement the testing of integrated circuits at the wafer-level under various resource constraints. Moreover, this unique book helps practitioners address the issue of enabling next generation products with previous generation testers. Practitioners also find expert insights on current industry trends in WLTBI test solutions.

Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as dynamic voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This book explores existing solutions for power-aware test and design-for-test of conventional circuits and systems, and surveys test strategies and EDA solutions for testing low power devices. Understanding the cost ramifications of design, manufacturing and life-cycle

management decisions is of central importance to businesses associated with all types of electronic systems. Cost Analysis of Electronic Systems contains carefully developed models and theory that practicing engineers can directly apply to the modeling of costs for real products and systems. In addition, this book brings to light and models many contributions to life-cycle costs that practitioners are aware of but never had the tools or techniques to address quantitatively in the past.Cost Analysis of Electronic Systems melds elements of traditional engineering economics with manufacturing process and life-cycle cost management concepts to form a practical foundation for predicting the cost of electronic products and systems. Various manufacturing cost analysis methods are addressed including: process-flow, parametric, cost of ownership, and activity-based costing. The effects of learning curves, data uncertainty, test and rework processes, and defects are considered. Aspects of system sustainment and life-cycle cost modeling including reliability (warranty, burn-in), maintenance (sparing and availability), and obsolescence are treated. Finally, total cost of ownership of systems and return on investment are addressed.Real life design scenarios from integrated circuit fabrication, electronic systems assembly, substrate fabrication, and electronic systems managementare used as examples of the application of the cost estimation methods developed within the book.

Model based testing is the most powerful technique for testing hardware and software systems. Models in Hardware Testing describes the use of models at all the levels of hardware testing. The relevant fault models for nanoscaled CMOS technology are introduced, and their implications on fault simulation, automatic test pattern generation, fault diagnosis, memory testing and power aware testing are discussed. Models and the corresponding algorithms are considered with respect to the most recent state of the art, and they are put into a historical context by a concluding chapter on the use of physical fault models in fault tolerance.

Are memory applications more critical than they have been in the past? Yes, but even more critical is the number of designs and the sheer number of bits on each design. It is assured that catastrophes, which were avoided in the past because memories were small, will easily occur if the design and test engineers do not do their jobs very carefully. High Performance Memory Testing: Design Principles, Fault Modeling and Self Test is based on the author's 20 years of experience in memory design, memory reliability development and memory self test. High Performance Memory Testing: Design Principles, Fault Modeling and Self Test is written for the professional and the researcher to help them understand the memories that are being tested.

This is a new type of edited volume in the Frontiers in Electronic Testing book series devoted to recent advances in electronic circuits testing. The book is a comprehensive elaboration on important topics which capture major research and development efforts today. "Hot" topics of current interest to test technology community have been selected, and the authors are key contributors in the corresponding topics.

SOC test design and its optimization is the topic of Introduction to Advanced System-on-Chip Test Design and Optimization. It gives an introduction to testing, describes the problems related to SOC testing, discusses the modeling granularity and the implementation into EDA (electronic design automation) tools. The book is divided into three sections: i) test concepts, ii) SOC design for test, and iii) SOC test applications. The first part covers an introduction into test problems including faults, fault types,

design-flow, design-for-test techniques such as scan-testing and Boundary Scan. The second part of the book discusses SOC related problems such as system modeling, test conflicts, power consumption, test access mechanism design, test scheduling and defect-oriented scheduling. Finally, the third part focuses on SOC applications, such as integrated test scheduling and TAM design, defect-oriented scheduling, and integrating test design with the core selection process.

Test Resource Partitioning for System-on-a-Chip is about test resource partitioning and optimization techniques for plug-and-play system-on-a-chip (SOC) test automation. Plug-and-play refers to the paradigm in which core-to-core interfaces as well as core-to-SOC logic interfaces are standardized, such that cores can be easily plugged into "virtual sockets" on the SOC design, and core tests can be plugged into the SOC during test without substantial effort on the part of the system integrator. The goal of the book is to position test resource partitioning in the context of SOC test automation, as well as to generate interest and motivate research on this important topic. SOC integrated circuits composed of embedded cores are now commonplace. Nevertheless, There remain several roadblocks to rapid and efficient system integration. Test development is seen as a major bottleneck in SOC design, and test challenges are a major contributor to the widening gap between design capability and manufacturing capacity. Testing SOCs is especially challenging in the absence of standardized test structures, test automation tools, and test protocols. Test Resource Partitioning for System-on-a-Chip responds to a pressing need for a structured methodology for SOC test automation. It presents new techniques for the partitioning and optimization of the three major SOC test resources: test hardware, testing time and test data volume. Test Resource Partitioning for System-on-a-Chip paves the way for a powerful integrated framework to automate the test flow for a large number of cores in an SOC in a plug-and-play fashion. The framework presented allows the system integrator to reduce test cost and meet short time-to-market requirements.

This book presents an overview of the issues related to the test, diagnosis and fault-tolerance of Network on Chip-based systems. It is the first book dedicated to the quality aspects of NoC-based systems and will serve as an invaluable reference to the problems, challenges, solutions, and trade-offs related to designing and implementing state-of-the-art, on-chip communication architectures.

A recent technological advance is the art of designing circuits to test themselves, referred to as a Built-In Self-Test. This book is written from a designer's perspective and describes the major BIST approaches that have been proposed and implemented, along with their advantages and limitations.

This book contains extended and revised versions of the best papers presented at the 26th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2018, held in Verona, Italy, in October 2018. The 13 full papers included in this volume were carefully reviewed and selected from the 27 papers (out of 106 submissions) presented at the conference. The papers discuss the latest academic and industrial results and developments as well as future trends in the field of System-on-Chip (SoC) design, considering the challenges of nano-scale, state-of-the-art and emerging manufacturing technologies. In particular they address cutting-edge research fields like heterogeneous, neuromorphic and brain-inspired, biologically-inspired, approximate computing systems.

As many circuits and applications now enter the Gigahertz frequency range, accurate digital timing measurements have become crucial in the design, verification, characterization, and application of electronic circuits. To be successful in this field an engineer needs to understand instrumentation, measurement techniques, signal integrity, jitter and timing concepts, and statistics. This book gives a compact, practice-oriented overview on all these subjects with emphasis on useable concepts and real-life guidelines.

This book provides an insightful guide to the design, testing and optimization of micro-electrode-dot-array (MEDA) digital microfluidic biochips. The authors focus on the characteristics specific for MEDA biochips, e.g., real-time sensing and advanced microfluidic operations like lamination mixing and droplet shape morphing. Readers will be enabled to enhance the automated design and use of MEDA and to develop a set of solutions to facilitate the full exploitation of design complexities that are possible with standard CMOS fabrication techniques. The book provides the first set of design automation and test techniques for MEDA biochips. The methods described in this book have been validated using fabricated MEDA biochips in the laboratory. Readers will benefit from an in-depth look at the MEDA platform and how to combine microfluidics with software, e.g., applying biomolecular protocols to software-controlled and cyberphysical microfluidic biochips.