Esd Basics From Semiconductor Manufacturing To Product Use

Provides the understanding and practical skills needed to develop and maintain an effective ESD control program for manufacturing, storage, and handling of ESD sensitive components This essential guide to ESD control programs explains the principles and practice of ESD control in an easily accessible way whilst also providing more depth and a wealth of references for those who want to gain a deeper knowledge of the subject. It describes static electricity and ESD principles such as triboelectrification, electrostatic fields, and induced voltages, with the minimum of theory or mathematics. It is designed for the reader to "dip into" as required, rather than need to read cover to cover. The ESD Control Program Handbook begins with definitions and commonly used terminology, followed by the principles of static electricity and ESD control. Chapter 3 discusses ESD susceptible electronic devices, and how ESD susceptibility of a component is measured. This is followed by the “Seven habits of a highly effective ESD program”, explaining the essential activities of an effective ESD control program. While most texts mainly address manual handling of ESD susceptible devices, Chapter 5 extends the discussion to ESD control in automated systems, processes and handling, which form a major part of modern electronic manufacture. Chapter 6 deals with requirements for compliance given by the IEC 61340-5-1 and ANSI/ESD S20.20 ESD control standards. Chapter 7 gives an overview of the selection, use, care and maintenance of equipment and furniture commonly used to control ESD risks. The chapter explains how these often work together as part of a system and must be specified with that in mind. ESD protective packaging is available in an extraordinary range of forms from bags, boxes and bubble wrap to tape and reel packaging for automated processes. The principles and practice of this widely misunderstood area of ESD control are introduced in Chapter 8. The thorny question of how to evaluate an ESD control program is addressed in Chapter 9 with a goal of compliance with a standard as well as effective control of ESD risks and possible customer perceptions. Whilst evaluating an existing ESD control program provides challenges, developing an ESD control program from scratch provides others. Chapter 10 gives an approach to this. Standard test methods used in compliance with ESD control standards are explained and simple test procedures given in Chapter 11. ESD Training has long been recognised as essential in maintaining effective ESD control. Chapter 12 discusses ways of covering essential topics and how to demonstrate static electricity in action. The book ends with a look at where ESD control may go in the near future. The ESD Control Program Handbook: Gives readers a sound understanding of the subject to analyze the ESD control requirements of manufacturing processes, and develop an effective ESD control program Provides practical knowledge, as well as sufficient theory and background to understand the principles of ESD control Teaches how to track and identify how ESD risks arise, and how to identify fitting means for minimizing or eliminating them Emphasizes working with modern ESD control program standards IEC 61340-5-1 and ESD S20:20 The ESD Control Program Handbook is an invaluable reference for anyone tasked with setting up, evaluating, or maintaining an effective ESD control program, training personnel, or making ESD control related measurements. It would form an excellent basis for a University course on the subject as well as a guide and resource for industry professionals.

Just as chemistry is a part of our daily lives, functional coatings can be found in almost every object, gadget or device you can see or touch. However, in the last 20 years the advances made in the preparation of different functional coatings with diverse compositions have allowed the development of nanoscale coatings that are more cost-effective and environmentally conscious than traditional coatings. Research Perspectives on Functional Micro- and Nanoscale Coatings highlights critical research on preparation methods, modification, organization, and utilization of functional coatings in micro, nano, and biotechnology. Emphasizing emerging developments and global research perspectives, this publication is a pivotal resource for engineers, researchers, and graduate-level students interested in learning about emerging developments in functional coatings and nanotechnology.

ESD Protection Device and Circuit Design for Advanced CMOS Technologies is intended for practicing engineers working in the areas of circuit design, VLSI reliability and testing domains. As the problems associated with ESD failures and yield losses become significant in the modern semiconductor industry, the demand for graduates with a basic knowledge of ESD is also increasing. Today, there is a significant demand to educate the circuits design and reliability teams on ESD issues. This book makes an attempt to address the ESD design and implementation in a systematic manner. A design procedure involving device simulators as well as circuit simulator is employed to optimize device and circuit parameters for optimal ESD as well as circuit performance. This methodology, described in ESD Protection Device and Circuit Design for Advanced CMOS Technologies has resulted in several successful ESD circuit design with excellent silicon results and demonstrates its strengths.

This book enables readers to design effective ESD protection solutions for all mainstream RF fabrication processes (GaAs pHEMT, SiGe HBT, CMOS). The new techniques introduced by the authors have much higher protection levels and much lower parasitic effects than those of existing ESD protection devices. The authors describe in detail the ESD phenomenon, as well as ESD protection fundamentals, standards, test equipment, and basic design strategies. Readers will benefit from realistic case studies of ESD protection for RFICs and will learn to increase significantly modern RFICs’ ESD safety level, while maximizing RF performance.

A comprehensive and in-depth review of analog circuitlayout, schematic architecture, device, power network and ESDdesign This book will provide a balanced overview of analog circuitdesign layout, analog circuit schematic development,architecture of chips, and ESD design. It will start atan introductory level and will bring the reader right up to thestate-of-the-art. Two critical design aspects for analog and powerintegrated circuits are combined. The first design aspect coversanalog circuit design techniques to achieve the desired circuitperformance. The second and main aspect presents the additionalchallenges associated with the design of adequate and effective ESDprotection elements and schemes. A comprehensive list of practicalapplication examples is used to demonstrate the successfulcombination of both techniques and any potential designtrade-offs. Chapter One looks at analog design discipline, including layoutand analog matching and analog layout design practices. Chapter Twodiscusses analog design with circuits, examining: singletransistor amplifiers; multi-transistor amplifiers; active loadsand more. The third chapter covers analog design layout (alsoMOSFET layout), before Chapters Four and Five discuss analog designsynthesis. The next chapters introduce the reader to analog-digitalmixed signal design synthesis, analog signal pin ESD networks, andanalog ESD power clamps. Chapter Nine, the last chapter, covers ESDdesign in analog applications. Clearly describes analog design fundamentals (circuitfundamentals) as well as outlining the various ESDimplications Covers a large breadth of subjects and technologies, such asCMOS, LDMOS, BCD, SOI, and thick body SOI Establishes an “ESD analog design” discipline thatdistinguishes itself from the alternative ESD digital designfocus Focuses on circuit and circuit design applications Assessible, with the artwork and tutorial style of the ESD bookseries PowerPoint slides are available for university facultymembers Even in the world of digital circuits, analog and power circuitsare two very important but under-addressed topics, especially fromthe ESD aspect. Dr. Voldman’s new book will serve as anessential and practical guide to the greater IC community. Withhigh practical and academic values this book is a“bible” for professionals, graduate students, deviceand circuit designers for investigating the physics of ESD and forproduct designs and testing.

Electrical Overstress (EOS) continues to impact semiconductor manufacturing, semiconductor components and systems as technologies scale from micro- to nano-electronics. This bookteaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures. The text provides a clear picture of EOS phenomena, EOS origins, EOS sources, EOS physics, EOS failure mechanisms,

and EOS on-chip and system design. It provides an illuminating insight into the sources of EOS in manufacturing, integration of on-chip, and system level EOS protection networks, followed by examples in specific technologies, circuits, and chips. The book is unique in covering the EOS manufacturing issues from on-chip design and electronic design automation to factory-level EOS program management in today's modern world. Look inside for extensive coverage on: Fundamentals of electrical overstress, from EOS physics, EOS time scales, safe operating area (SOA), to physical models for EOS phenomena EOS sources in today's semiconductor manufacturing environment, and EOS program management, handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices, circuits and system Discussion of how to distinguish between EOS events, and electrostatic discharge (ESD) events (e.g. such as human body model (HBM), charged device model (CDM), cable discharge events (CDM), charged board events (CBE), to system level IEC 61000-4-2 test events) EOS protection on-chip design practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards (PCB), and manufacturing equipment Examples of EOS issues in state-of-the-art digital, analog and power technologies including CMOS, LDMOS, and BCD EOS design rule checking (DRC), LVS, and ERC electronic design automation (EDA) and how it is distinct from ESD EDA systems EOS testing and qualification techniques, and Practical off-chip ESD protection and system level solutions to provide more robust systems Electrical Overstress (EOS): Devices, Circuits and Systems is a continuation of the author's series of books on ESD protection. It is an essential reference and a useful insight into the issues that confront modern technology as we enter the nano-electronic era.

Electrostatic Discharge is a pervasive issue in the semiconductor industry affecting both manufacturers and users of semiconductors. This easy-to-read, practical handbook presents an overview of ESD as it effects electronic circuits and provides a concise introduction for students, engineers, circuit designers and failure analysts.

Materials and products designed to lessen the impact of static electricity represent a relatively mature market, but one in which new opportunities are beginning to emerge. On the demand side, increased miniaturization of PCBs and hard drives coupled with ever smaller devices on computer chips will increase the threats of damage and costs caused by static electricity; we believe that this will provide the ESD products and coatings market with growth for years to come.Antistatic concerns are also growing at both the manufacturing and packaging levels. At the same time, technological improvements in ESD coatings are to be expected, especially in the vibrant areas of nanomaterials and conductive polymers.In this report, NanoMarkets will identify and quantify the new opportunities in ESD products and materials that are emerging as a result of the increased antistatic concerns discussed above. This report is a follow-on report from the well-received industry analysis on antistatic coatings that NanoMarkets carried out for its conductive coatings market study published last year. In this report, we extend the coverage across the entire ESD/antistatic product and material value chain to include not just basic materials but also laminates, films and other materials, as well higher value products such as bags, garments and flooring.

Now you can navigate the complex legal world of international securities and derivatives with this all-new fifth edition of an expert guide to today's global financial markets. You'll find clear analysis of the legal framework for all types of cross-border securities offerings by U.S. and non-U.S, issuers -- from U.S. registered ADR programs and private offerings to international issues and highly structured instruments. U.S. Regulation of the International Securities and Derivatives Markets offers authoritative answers to just about any question you'll face on such topics as: Recent legal developments, including the Gramm-Leach-Bliley Act on financial modernization -- New initiatives by the SEC, the Federal Reserve Board and the CFTC to facilitate the increasing pace of cross-border activity -- The distribution of securities outside the U.S -- How foreign companies can access U.S. capital markets -- How U.S. regulations affect foreign issuers of securities traded in the U.S. -- New trends in private offerings and the effect of Rule 144A -- How public offerings of securities made abroad can be exempt from registration requirements of the Securities Act -- How the U.S. regulates investment advisers -- How foreign banks and their affiliates doing business with the U.S. are regulated -- How various categories of derivative instruments are classified under U.S. securities and commodities laws -- And much more.

A practical guide to the effects of radiation on semiconductor components of electronic systems, and techniques for the designing, laying out, and testing of hardened integrated circuits This book teaches the fundamentals of radiation environments and their effects on electronic components, as well as how to design, lay out, and test cost-effective hardened semiconductor chips not only for today's space systems but for commercial terrestrial applications as well. It provides a historical perspective, the fundamental science of radiation, and the basics of semiconductors, as well as radiation-induced failure mechanisms in semiconductor chips. Integrated Circuits Design for Radiation Environments starts by introducing readers to semiconductors and radiation environments (including space, atmospheric, and terrestrial environments) followed by circuit design and layout. The book introduces radiation effects phenomena including single-event effects, total ionizing dose damage and displacement damage) and shows how technological solutions can address both phenomena. Describes the fundamentals of radiation environments and their effects on electronic components Teaches readers how to design, lay out and test cost-effective hardened semiconductor chips for space systems and commercial terrestrial applications Covers natural and man-made radiation environments, space systems and commercial terrestrial applications Provides up-to-date coverage of state-of-the-art of radiation hardening technology in one concise volume Includes questions and answers for the reader to test their knowledge Integrated Circuits Design for Radiation Environments will appeal to researchers and product developers in the semiconductor, space, and defense industries, as well as electronic engineers in the medical field. The book is also helpful for system, layout, process, device, reliability, applications, ESD, latchup and circuit design semiconductor engineers, along with anyone involved in micro-electronics used in harsh environments.

The design and study of materials is a pivotal component to new discoveries in the various fields of science and technology. By better understanding the components and structures of materials, researchers can increase its applications across different industries. Materials Science and Engineering: Concepts, Methodologies, Tools, and Applications is a compendium of the latest academic material on investigations, technologies, and techniques pertaining to analyzing the synthesis and design of new materials.

Through its broad and extensive coverage on a variety of crucial topics, such as nanomaterials, biomaterials, and relevant computational methods, this multi-volume work is an essential reference source for engineers, academics, researchers, students, professionals, and practitioners seeking innovative perspectives in the field of materials science and engineering.

With the evolution of semiconductor technology and global diversification of the semiconductor business, testing of semiconductor devices to systems for electrostatic discharge (ESD) and electrical overstress (EOS) has increased in importance. ESD Testing: From Components to Systems updates the reader in the new tests, test models, and techniques in the characterization of semiconductor components for ESD, EOS, and latchup. Key features: Provides understanding and knowledge of ESD models and specifications including human body model (HBM), machine model (MM), charged device model (CDM), charged board model (CBM), cable discharge events (CDE), human metal model (HMM), IEC 61000-4-2 and IEC 61000-4-5. Discusses new testing methodologies such as transmission line pulse (TLP), to very fast transmission line pulse (VF-TLP), and future methods of long pulse TLP, to ultra-fast TLP (UF-TLP). Describes both conventional testing and new testing techniques for both chip and system level evaluation. Addresses EOS testing, electromagnetic compatibility (EMC) scanning, to current reconstruction methods. Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing. ESD Testing: From Components to Systems is part of the authors' series of books on electrostatic discharge (ESD) protection; this book will be an invaluable reference for the professional semiconductor chip and system-level ESD and EOS test engineer. Semiconductor device and process development, circuit designers, quality, reliability and failure analysis engineers will also find it an essential reference. In addition, its academic treatment will appeal to both senior and graduate students with interests in semiconductor process, device physics, semiconductor testing and experimental work.

This fourth edition of the book provides readers with a detailed explanation of PLM, enabling them to gain a full understanding and the know-how to implement PLM within their own business environment. This new and expanded edition has been fully updated to reflect the numerous technological and management advances made in PLM since the release of the third edition in 2014, including chapters on both the Internet of Things and Industry 4.0. The book describes the environment in which products are ideated, developed, manufactured, supported and retired before addressing the main components of PLM and PLM Initiatives. These include product-related business processes, product data, product data management (PDM) systems, other PLM applications, best practices, company objectives and organisation. Key activities in PLM Initiatives include Organisational Change Management (OCM) and Project Management. Lastly, it addresses the PLM Initiative, showing the typical steps and activities of a PLM project or initiative. Enhancing readers' understanding of PLM, the book enables them to develop the skills needed to implement PLM successfully and achieve world-class product performance across the lifecycle.

An effective and cost efficient protection of electronic system against ESD stress pulses specified by IEC 61000-4-2 is paramount for any system design. This pioneering book presents the collective knowledge of system designers and system testing experts and state-of-the-art techniques for achieving efficient system-level ESD protection, with minimum impact on the system performance. All categories of system failures ranging from 'hard' to 'soft' types are considered to review simulation and tool applications that can be used. The principal focus of System Level ESD Co-Design is defining and establishing the importance of co-design efforts from both IC supplier and system builder perspectives. ESD designers often face challenges in meeting customers' system-level ESD requirements and, therefore, a clear understanding of the techniques presented here will facilitate effective simulation approaches leading to better solutions without compromising system performance. With contributions from Robert Ashton, Jeffrey Dunnihoo, Micheal Hopkins, Pratik Maheshwari, David Pomerenke, Wolfgang Reinprecht, and Matti Usumaki, readers benefit from hands-on experience and in-depth knowledge in topics ranging from ESD design and the physics of system ESD phenomena to tools and techniques to address soft failures and strategies to design ESD-robust systems that include mobile and automotive applications. The first dedicated resource to system-level ESD co-design, this is an essential reference for industry ESD designers, system builders, IC suppliers and customers and also Original Equipment Manufacturers (OEMs). Key features: Clarifies the concept of system level ESD protection. Introduces a co-design approach for ESD robust systems. Details soft and hard ESD fail mechanisms. Detailed protection strategies for both mobile and automotive applications. Explains simulation tools and methodology for system level ESD co-design and overviews available test methods and standards. Highlights economic benefits of system ESD co-design.

The international market is very competitive for high-tech manufacturers to day. Achieving competitive quality and reliability for products requires leader ship from the top, good management practices, effective and efficient operation and maintenance systems, and use of appropriate up-to-date engineering de sign tools and methods. Furthermore, manufacturing yield and reliability are interrelated. Manufacturing yield depends on the number of defects found dur ing both the manufacturing process and the warranty period, which in turn determines the reliability. the production of microelectronics has evolved into Since the early 1970's, one of the world's largest manufacturing industries. As a result, an important agenda is the study of reliability issues in fabricating microelectronic products and consequently the systems that employ these products, particularly, the new generation of microelectronics. Such an agenda should include: • the economic impact of employing the microelectronics fabricated by in dustry, • a study of the relationship between reliability and yield, • the progression toward miniaturization and higher reliability, and • the correctness and complexity of new system designs, which include a very significant portion of software.

The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high-performance chips and portable devices. The study of power-saving design methodologies now must also include subjects such as systems on chips, embedded software, and the future of microelectronics. Low-Power Electronics Design covers all major aspects of low-power design of ICs in deep submicron technologies and addresses emerging topics related to future design. This volume explores, in individual chapters written by expert authors, the many low-power techniques born

during the past decade. It also discusses the many different domains and disciplines that impact power consumption, including processors, complex circuits, software, CAD tools, and energy sources and management. The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality. They investigate nanotechnologies, optical circuits, ad hoc networks, e-textiles, as well as human powered sources of energy. Low-Power Electronics Design delivers a complete picture of today's methods for reducing power, and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now.

This volume presents an integrated treatment of ESD, I/O, and process parameter interactions that both I/O designers and process designers can use. It examines key factors in I/O and ESD design and testing, and helps the reader consider ESD and reliability issues up front when making I/O choices. Emphasizing clarity and simplicity, this book focuses on design principles that can be applied widely as this dynamic field continues to evolve.

Electrostatic discharge (ESD) is defined as the transfer of charge between bodies at different potentials. The electrostatic discharge induced integrated circuit damages occur throughout the whole life of a product from the manufacturing, testing, shipping, handing, to end user operating stages. This is particularly true as microelectronics technology continues shrink to nano-metric dimensions. The ESD related failures is a major IC reliability concern and results in a loss of millions dollars to the semiconductor industry each year. Several ESD stress models and test methods have been developed to reproduce the real world ESD discharge events and quantify the sensitivity of ESD protection structures. The basic ESD models are: Human body model (HBM), Machine model (MM), and Charged device model (CDM). To avoid or reduce the IC failure due to ESD, the on-chip ESD protection structures and schemes have been implemented to discharge ESD current and clamp overstress voltage under different ESD stress events. Because of its simple structure and good performance, the junction diode is widely used in on-chip ESD protection applications. This is particularly true for ESD protection of low-voltage ICs where a relatively low trigger voltage for the ESD protection device is required. However, when the diode operates under the ESD stress, its current density and temperature are far beyond the normal conditions and the device is in danger of being damaged. For the design of effective ESD protection solution, the ESD robustness and low parasitic capacitance are two major concerns. The ESD robustness is usually defined after the failure current It2 and on-state resistance Ron. The transmission line pulsing (TLP) measurement is a very effective tool for evaluating the ESD robustness of a circuit or single element. This is particularly helpful in characterizing the effect of HBM stress where the ESD-induced damages are more likely due to thermal failures. Two types of diodes with different anode/cathode isolation technologies will be investigated for their ESD performance: one with a LOCOS (Local Oxidation of Silicon) oxide isolation called the LOCOS-bound diode, the other with a polysilicon gate isolation called the polysilicon-bound diode. We first examine the ESD performance of the LOCOS-bound diode. The effects of different diode geometries, metal connection patterns, dimensions and junction configurations on the ESD robustness and parasitic capacitance are investigated experimentally. The devices considered are N+/P-well junction LOCOS-bound diodes having different device widths, lengths and finger numbers, but the approach applies generally to the P+/N-well junction diode as well. The results provide useful insights into optimizing the diode for robust HBM ESD protection applications. Then, the current carrying and voltage clamping capabilities of LOCOS- and polysilicon-bound diodes are compared and investigated based on both TCAD simulation and experimental results. Comparison of these capabilities leads to the conclusion that the polysilicon-bound diode is more suited for ESD protection applications due to its higher performance. The effects of polysilicon-bound diode's design parameters, including the device width, anode/cathode length, finger number, poly-gate length, terminal connection and metal topology, on the ESD robustness are studied. Two figures of merits, FOM_It2 and FOM_Ron, are developed to better assess the effects of different parameters on polysilicon-bound diode's overall ESD performance. As latest generation package styles such as mBGAs, SOTs, SC70s, and CSPs are going to the millimeter-range dimensions, they are often effectively too small for people to handle with fingers. The recent industry data indicates the charged device model (CDM) ESD event becomes increasingly important in today's manufacturing environment and packaging technology. This event generates highly destructive pulses with a very short rise time and very small duration. TLP has been modified to probe CDM ESD protection effectiveness. The pulse width was reduced to the range of 1-10 ns to mimic the very fast transient of the CDM pulses. Such a very fast TLP (VFTLP) testing has been used frequently for CDM ESD characterization. The overshoot voltage and turn-on time are two key considerations for designing the CDM ESD protection devices. A relatively high overshoot voltage can cause failure of the protection devices as well as the protected devices, and a relatively long turn-on time may not switch on the protection device fast enough to effectively protect the core circuit against the CDM stress. The overshoot voltage and turn-on time of an ESD protection device can be observed and extracted from the voltage versus time waveforms measured from the VFTLP testing. Transient behaviors of polysilicon-bound diodes subject to pulses generated by the VFTLP tester are characterized for fast ESD events such as the charged device model. The effects of changing devices' dimension parameters on the transient behaviors and on the overshoot voltage and turn-on time are studied. The correlation between the diode failure and poly-gate configuration under the VFTLP stress is also investigated. Silicon-controlled rectifier (SCR) is another widely used ESD device for protecting the I/O pins and power supply rails of integrated circuits. Multiple fingers are often needed to achieve optimal ESD protection performance, but the uniformity of finger triggering and current flow is always a concern for multi-finger SCR devices operating under the post-snapback region. Without a proper understanding of the finger turn-on mechanism, design and realization of robust SCRs for ESD protection applications are not possible. Two two-finger SCRs with different combinations of anode/cathode regions are considered, and their finger turn-on uniformities are analyzed based on the I-V characteristics obtained from the transmission line pulsing (TLP) tester. The dV/dt effect of pulses with different rise times on the finger turn-on behavior of the SCRs are also investigated experimentally. In this work, unless noted otherwise, all the measurements are conducted using the Barth 4002 transmission line pulsing (TLP) and Barth 4012 very-fast transmission line pulsing (VFTLP) testers.

ESD BasicsFrom Semiconductor Manufacturing to Product UseJohn Wiley & Sons

In today's electronics business, managing an ESD progranris an integral part of a complete quality program. In fact, any electronics firm without an active ESD program puts itself and its customers at risk. This book illustrates one good example of the detail and dedication to quality that AT&T expects within its own operations and from its suppliers. Writing of the book began at a time when Ted Dangelmayer was burdened with many demands. These demands were from AT&T's own operations, internal suppliers, external suppliers, customers and others looking for a better understanding of the phenomenon of ESD, its impact and, most of all, ways to control and manage it. In a way, this book is a response to these demands by making available a reader friendly document that distills the hard-won experiences of Ted and AT&T. The information and methods in this book have been gained at no small cost and produce results that far exceed eXRenses. There is, however, a caveat: Success will not be obtained unless there is real management commitment. This means management must allocate the necessary resources and provide active support to ensure that training, auditing, reporting, tracking and an aggressive corrective action program all take place successfully. Ted is an internationally recognized authority, and you will benefit greatly by listening to his advice and following his recommendations.

As we enter the nanoelectronics era, electrostatic discharge (ESD) phenomena is an important issue for everything from micro-electronics to nanostructures. This book provides insight into the operation and design of micro-gaps and nanogenerators with chapters on low capacitance ESD design in advanced technologies, electrical breakdown in micro-gaps, nanogenerators from ESD, and theoretical prediction and optimization of triboelectric nanogenerators. The information contained herein will prove useful for for engineers and scientists that have an interest in ESD physics and design.

A practical "how to" guide that effectively deals with the control of both contamination and ESD This book offers effective strategies and techniques for contamination and electrostatic discharge (ESD) control that can be implemented in a wide range of high-technology industries, including semiconductor, disk drive, aerospace, pharmaceutical, medical device, automobile, and food production manufacturing. The authors set forth a new and innovative methodology that can manage both contamination and ESD, often considered to be mutually exclusive challenges requiring distinct strategies. Beginning with two general chapters on the fundamentals of contamination and ESD control, the book presents a logical progression of topics that collectively build the necessary skills and knowledge: Analysis methods for solving contamination and ESD problems Building the contamination and ESD control environment, including design and construction of cleanrooms and ESD protected environments Cleaning processes and the equipment needed to support these processes Tooling design and certification Continuous monitoring Consumable supplies and packaging materials Controlling contamination and ESD originating from people Management of cleanrooms and ESD protected workplace environments Contamination and ESD Control in High-Technology Manufacturing conveys a practical, working knowledge of contamination and ESD control strategies and techniques, and it is filled with case studies that illustrate key principles and the benefits of contamination and ESD control. Moreover, its straightforward style makes the material, which integrates many disciplines of engineering and science, clear and accessible. Written by three leading industry experts, this book is an essential guide for engineers and designers across the many industries where contamination and ESD control is a concern.

This handbook will provide engineers with the principles, applications, and solutions needed to design and manage semiconductor manufacturing operations. Consolidating the many complex fields of semiconductor fundamentals and manufacturing into one volume by deploying a team of world class specialists, it allows the quick look up of specific manufacturing reference data across many subdisciplines.

This book provides a system-level approach to making packaging decisions for millimeter-wave transceivers. In electronics, the packaging forms a bridge between the integrated circuit or individual device and the rest of the electronic system, encompassing all technologies between the two. To be able to make well-founded packaging decisions, researchers need to understand a broad range of aspects, including: concepts of transmission bands, antennas and propagation, integrated and discrete package substrates, materials and technologies, interconnects, passive and active components, as well as the advantages and disadvantages of various packages and packaging approaches, and package-level modeling and simulation. Packaging also needs to be considered in terms of system-level testing, as well as associated testing and production costs, and reducing costs. This peer-reviewed work contributes to the extant scholarly literature by addressing the aforementioned concepts and applying them to the context of the millimeter-wave regime and the unique opportunities that this transmission approach offers.

"Electrostatic discharge (ESD)"--Page xxi.

The book all semiconductor device engineers must read to gain a practical feel for latchup-induced failure to produce lower-cost and higher-density chips. Transient-Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout. Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup, explaining the critical issues that have resurfaced for CMOS technologies. Once readers can gain an understanding of the standard practices for TLU, Ker and Hsu discuss the physical mechanism of TLU under a system-level ESD test, while introducing an efficient component-level TLU measurement setup. The authors then present experimental methodologies to extract safe and area-efficient compact layout rules for latchup prevention, including layout rules for I/O cells, internal circuits, and between I/O and internal circuits. The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0.18-micrometer 1.8V/3.3V silicided CMOS process. Presents real cases and solutions that occur in commercial CMOS IC chips Equips engineers with the skills to conserve chip layout area and decrease time-to-market Written by experts with real-world experience in circuit design and failure analysis Distilled from numerous courses taught by the authors in IC design houses worldwide The only book to introduce TLU under system-level ESD and EFT tests This book is essential for practicing engineers involved in IC design, IC design management, system and application design, reliability, and failure analysis. Undergraduate and postgraduate students, specializing in CMOS circuit design and layout, will find this book to be a valuable introduction to real-world industry problems and a key reference during the course of their careers.

This book provides readers with a broad overview of integrated circuits, also generally referred to as micro-electronics. The presentation is designed to be accessible to readers with limited, technical knowledge and coverage includes key aspects of integrated circuit design, implementation, fabrication and application. The author complements his discussion with a large number of diagrams and photographs, in order to reinforce the explanations. The book is divided into two parts, the first of which is specifically developed for people with almost no or little technical knowledge. It presents an overview of the electronic evolution and discusses the similarity between a chip floor plan and a city plan, using metaphors to help explain concepts. It includes a summary of the chip development cycle, some basic definitions and a variety of applications that use integrated circuits. The second part digs deeper into the details and is perfectly suited for professionals working in one of the semiconductor disciplines who want to broaden their semiconductor horizon.

Electrostatic discharge (ESD) continues to impact semiconductormanufacturing, semiconductor components and systems, astechnologies scale from micro- to nano electronics. This bookintroduces the fundamentals of ESD, electrical overstress (EOS),electromagnetic interference (EMI), electromagnetic compatibility(EMC), and latchup, as well as

provides a coherent overview of thesemiconductor manufacturing environment and the final systemassembly. It provides an illuminating look into the integration ofESD protection networks followed by examples in specifictechnologies, circuits, and chips. The text is unique in covering semiconductor chip manufacturingissues, ESD semiconductor chip design, and system problemsconfronted today as well as the future of ESD phenomena andnano-technology. Look inside for extensive coverage on: The fundamentals of electrostatics, triboelectric charging, andhow they relate to present day manufacturing environments ofmicro-electronics to nano-technology Semiconductor manufacturing handling and auditing processing toavoid ESD failures ESD, EOS, EMI, EMC, and latchup semiconductor component andsystem level testing to demonstrate product resilience from humanbody model (HBM), transmission line pulse (TLP), charged devicemodel (CDM), human metal model (HMM), cable discharge events (CDE),to system level IEC 61000-4-2 tests ESD on-chip design and process manufacturing practices andsolutions to improve ESD semiconductor chip solutions, alsopractical off-chip ESD protection and system level solutions toprovide more robust systems System level concerns in servers, laptops, disk drives, cellphones, digital cameras, hand held devices, automobiles, and spaceapplications Examples of ESD design for state-of-the-art technologies,including CMOS, BiCMOS, SOI, bipolar technology, high voltage CMOS(HVCMOS), RF CMOS, smart power, magnetic recording technology,micro-machines (MEMs) to nano-structures ESD Basics: From Semiconductor Manufacturing to ProductUse complements the author’s series of books on ESDprotection. For those new to the field, it is an essentialreference and a useful insight into the issues that confront moderntechnology as we enter the Nano-electronic Era.

An authoritative single-volume reference on the design and testing of electrostatic discharge (ESD) structures Electrostatic discharge (ESD) is a serious challenge to the reliability of semiconductors, integrated circuits (ICs), and microelectronic systems—on-chip ESD protection is a vital component of smartphones, laptops, tablets, and other electronic devices. Practical ESD Protection Design provides comprehensive and systematic guidance on all major aspects of on-chip ESD protection for integrated circuits (ICs). Written for students and practicing engineers alike, this one-stop resource covers essential theories, hands-on design skills, computer-aided design (CAD) methods, ESD failure testing and analysis, and more. Detailed chapters examine an array of topics ranging from fundamental to advanced, including ESD phenomena, ESD protection devices and circuits, ESD design layout and technology effects, emerging ESD protection designs, and circuit simulation modelling. Based on the author’s decades of design, teaching, and research experience, Practical ESD Protection Design: Features numerous real-world examples of electrostatic discharge (ESD) protection designs and skills Describes the design methodology for high-performance mixed-signal ICs and broadband radio-frequency (RF) ICs Discusses CAD-based ESD protection design using existing tools such as Technology Computer-Aided Design (TCAD) and SPICE simulation Addresses new ESD CAD algorithms and tools for full-chip ESD physical design verification Explores the disruptive future outlook of ESD protection Practical ESD Protection Design is a valuable reference for industrial engineers and academic researchers in the field, and an excellent textbook for electronic engineering courses in semiconductor microelectronics and integrated circuit design.

In two volumes, Planning Production and Inventories in the Extended Enterprise: A State of the Art Handbook examines production planning across the extended enterprise against a backdrop of important gaps between theory and practice. The early chapters describe the multifaceted nature of production planning problems and reveal many of the core complexities. The middle chapters describe recent research on theoretical techniques to manage these complexities. Accounts of production planning system currently in use in various industries are included in the later chapters. Throughout the two volumes there are suggestions on promising directions for future work focused on closing the gaps.

This book examines ways in which formerly prosperous regions can renew their economy during and after a period of industrial and economic recession. Using New York’s Capital Region (i.e., Albany, Troy, Schenectady, etc.) as a case study, the authors show how entrepreneurship, innovation, investment in education, research and political collaboration are critical to achieving regional success. In this way, the book provides other regions and nations with a real-life model for successful economic development. In the past half century, the United States and other nations have seen an economic decline of formerly prosperous regions as a result of new technology and globalization. One of the hardest-hit United States regions is Upstate New York or “the Capital Region”; it experienced a demoralizing hemorrhage of manufacturing companies, jobs and people to other regions and countries. To combat this, the region, with the help of state leaders, mounted a decades-long effort to renew and restore the region’s economy with a particular focus on nanotechnology. As a result, New York’s Capital Region successfully added thousands of well-paying, skill-intensive manufacturing jobs. New York’s success story serves as a model for economic development for policy makers that includes major public investments in educational institutions and research infrastructure; partnerships between academia, industry and government; and creation of frameworks for intra-regional collaboration by business, government, and academic actors. Featuring recommendations for best practices in regional development policy, this book is appropriate for scholars, students, researchers and policy makers in regional development, innovation, R&D policy, economic development and economic growth.

A practical and comprehensive reference that explores Electrostatic Discharge (ESD) in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems. Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection. Written by a noted expert on the topic, the text offers a topic-by-topic reference that includes illustrative figures, discussions, and drawings. The handbook covers a wide-range of topics including ESD in manufacturing (garments, wrist

straps, and shoes); ESD Testing; ESD device physics; ESD semiconductor process effects; ESD failure mechanisms; ESD circuits in different technologies (CMOS, Bipolar, etc.); ESD circuit types (Pin, Power, Pin-to-Pin, etc.); and much more. In addition, the text includes a glossary, index, tables, illustrations, and a variety of case studies. Contains a well-organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians, operators, engineers, circuit designers, and failure analysis engineers, The ESD Handbook contains an accessible reference to ESD design and ESD systems.

The power consumption of microprocessors is one of the most important challenges of high-performance chips and portable devices. In chapters drawn from Piguet's recently published Low-Power Electronics Design, Low-Power CMOS Circuits: Technology, Logic Design, and CAD Tools addresses the design of low-power circuitry in deep submicron technologies. It provides a focused reference for specialists involved in designing low-power circuitry, from transistors to logic gates. The book is organized into three broad sections for convenient access. The first examines the history of low-power electronics along with a look at emerging and possible future technologies. It also considers other technologies, such as nanotechnologies and optical chips, that may be useful in designing integrated circuits. The second part explains the techniques used to reduce power consumption at low levels. These include clock gating, leakage reduction, interconnecting and communication on chips, and adiabatic circuits. The final section discusses various CAD tools for designing low-power circuits. This section includes three chapters that demonstrate the tools and low-power design issues at three major companies that produce logic synthesizers. Providing detailed examinations contributed by leading experts, Low-Power CMOS Circuits: Technology, Logic Design, and CAD Tools supplies authoritative information on how to design and model for high performance with low power consumption in modern integrated circuits. It is a must-read for anyone designing modern computers or embedded systems.