Design For High Performance Low Power And Reliable 3d Integrated Circuits

Modeling and Simulation of Mixed Analog-Digital Systems brings together in one place important contributions and state-of-the-art research results in this rapidly advancing area. Modeling and Simulation of Mixed Analog-Digital Systems serves as an excellent reference, providing insight into some of the most important issues in the field.

Investigating the logic, conduct and nature of war on the highest political and strategic levels, these essays put less emphasis on operational and tactical aspects. They look at the impact of technology on warfare, the political nature of war and the limits of rational analysis in studying war.

This book introduces the state-of-the-art in research in parallel and distributed embedded systems, which have been enabled by developments in silicon technology, micro-electro-mechanical systems (MEMS), wireless communications, computer networking, and digital electronics. These systems have diverse applications in domains including military and defense, medical, automotive, and unmanned autonomous vehicles. The emphasis of the book is on the modeling and optimization of emerging parallel and distributed embedded systems in relation to the three key design metrics of performance, power and dependability. Key features: Includes an embedded wireless sensor networks case study to help illustrate the modeling and optimization of distributed embedded systems. Provides an analysis of multi-core/many-core based embedded systems to explain the modeling and optimization of parallel embedded systems. Features an application metrics estimation model; Markov modeling for fault tolerance and analysis; and queueing theoretic modeling for performance evaluation. Discusses optimization approaches for distributed wireless sensor networks; high-performance and energy-efficient techniques at the architecture, middleware and software levels for parallel multicore-based embedded systems; and dynamic optimization methodologies. Highlights research challenges and future research directions. The book is primarily aimed at researchers in embedded systems; however, it will also serve as an invaluable reference to senior undergraduate and graduate students with an interest in embedded systems research.

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This book describes the optimized implementations of several arithmetic datapath, controlpath and pseudorandom sequence generator circuits for realization of high performance arithmetic circuits targeted towards a specific family of the high-end Field Programmable Gate Arrays (FPGAs). It explores regular, modular, cascadable and bit-sliced architectures of these circuits, by directly instantiating the target FPGA-specific primitives in the HDL. Every proposed architecture is justified with detailed mathematical analyses.

Simultaneously, constrained placement of the circuit building blocks is performed, by placing the logically related hardware primitives in close proximity to one another by supplying relevant placement constraints in the Xilinx proprietary “User Constraints File”. The book covers the implementation of a GUI-based CAD tool named FlexiCore integrated with the Xilinx Integrated Software Environment (ISE) for design automation of platform-specific high-performance arithmetic circuits from user-level specifications. This tool has been used to implement the proposed circuits, as well as hardware implementations of integer arithmetic algorithms where several of the proposed circuits are used as building blocks. Implementation results demonstrate higher performance and superior operand-width scalability for the proposed circuits, with respect to implementations derived through other existing approaches. This book will prove useful to researchers, students and professionals engaged in the domain of FPGA circuit optimization and implementation.

Designing Stress Resistant Organizations demonstrates, in a persuasive way, how computational organization theory can be applied to advance the field of management with its successful integration of theory and practice. At the theoretical level, the book contains a comprehensive computational framework called DYCORP, which simulates dynamic and interactive organizational behaviors by incorporating multiple factors such as organizational design, task environment, and stress, and which generates consistent and insightful propositions on organizational performance. The book utilizes an organization science based approach to computational modeling. This approach recognizes the limit of human cognition as it was outlined by Herbert A. Simon in 1947. The model strives to focus on the essence of the reality that is most relevant to the research issue. This approach has been proven to be more beneficial for us to understand the underlying dynamics of the phenomenon.

This book constitutes the refereed proceedings of the Third International Conference on High Performance Computing and Communications, HPCC 2007. The 75 revised full papers address all current issues of parallel and distributed systems and high performance computing and communication, including networking protocols, embedded systems, wireless, mobile and pervasive computing, Web services and internet computing, and programming interfaces for parallel systems.

Chip Design and Implementation from a Practical Viewpoint Focusing on chip implementation, Low-Power NoC for High-Performance SoC Design provides practical knowledge and real examples of how to use network on chip (NoC) in the design of system on chip (SoC). It discusses many architectural and theoretical studies on NoCs, including design methodology, topology exploration, quality-of-service guarantee, low-power design, and implementation trials. The Steps to Implement NoC The book covers the full spectrum of the subject, from theory to actual chip design using NoC. Employing the Unified Modeling Language (UML) throughout, it presents complicated concepts, such as models

of computation and communication–computation partitioning, in a manner accessible to laypeople. The authors provide guidelines on how to simplify complex networking theory to design a working chip. In addition, they explore the novel NoC techniques and implementations of the Basic On-Chip Network (BONE) project. Examples of real-time decisions, circuit-level design, systems, and chips give the material a real-world context. Low-Power NoC and Its Application to SoC Design Emphasizing the application of NoC to SoC design, this book shows how to build the complicated interconnections on SoC while keeping a low power consumption.

This book constitutes the refereeds proceedings of the International Conference on High Performance Architecture and Grid Computing, HPAGC 2011, held in Chandigarh, India, in July 2011. The 87 revised full papers presented were carefully reviewed and selected from 240 submissions. The papers are organized in topical sections on grid and cloud computing; high performance architecture; information management and network security.

Because of their widespread use in mainframes, PCs, and mobile audio and video devices, DRAMs are being manufactured in ever increasing volume, both in stand-alone and in embedded form as part of a system on chip. Due to the optimum design of their components—access transistor, storage capacitor, and peripherals—DRAMs are the cheapest and densest semiconductor memory currently available. As a result, most of DRAM structure research and development focuses on the technology used for its constituent components and their interconnections. However, only a few books are available on semiconductor memories in general and fewer on DRAMs. Dynamic RAM: Technology Advancements provides a holistic view of the DRAM technology with a systematic description of the advancements in the field since the 1970s, and an analysis of future challenges. Topics Include: DRAM cells of all types, including planar, three-dimensional (3-D) trench or stacked, COB or CUB, vertical, and mechanically robust cells using advanced transistors and storage capacitors Advancements in transistor technology for the RCAT, SCAT, FinFET, BT FinFET, Saddle and advanced recess type, and storage capacitor realizations How sub 100 nm trench DRAM technologies and sub 50 nm stacked DRAM technologies and related topics may lead to new research Various types of leakages and power consumption reduction methods in active and sleep mode Various types of SAs and yield enhancement techniques employing ECC and redundancy A worthwhile addition to semiconductor memory research, academicians and researchers interested in the design and optimization of high-density and cost-efficient DRAMs may also find it useful as part of a graduate-level course.

Maintaining the United States' strong lead in information technology will require continued federal support of research in this area, most of which is currently funded under the High Performance Computing and Communications Initiative (HPCCI). The Initiative has already accomplished a great deal and should be continued. This book provides 13 major recommendations for refining both HPCCI and support of information technology research in general. It also provides a good overview of the development of HPCC technologies.

Presents information in a user-friendly, easy-access way so that the book can act as either a quick reference for more experienced engineers or as an introductory guide for new engineers and college graduates.

The design and implementation of a crypto processor based on Cryptographic algorithms can be used in wide range of electronic devices, include PCs, PDAs, hardware security modules, web servers etc. The growing problem of breaches in information security in recent years has created a demand for earnest efforts towards ensuring security in electronic processors. The successful deployment of these

electronic processors for ecommerce, Internet banking, government online services, VPNs, mobile commerce etc., are dependent on the effectiveness of the security solutions. These security concerns are further compounded when resource-constrained environments and real-time speed requirements have to be considered in next generation applications. Consequently, these IT and Network security issues have been a subject of intensive research in areas of computing, networking and cryptography these last few years. Computational methodologies, computer arithmetic, and encryption algorithms need deep investigation and research to obtain efficient integrations of crypto-processors, with desirable improvements and optimizations. Approaches on silicon achieve high values of speed and bandwidth.

This book constitutes the thoroughly refereed post-conference proceedings of the 5th International Conference on Mobile, Secure and Programmable Networking, held in Mohammedia, Morocco, in April 2019. The 23 papers presented in this volume were carefully reviewed and selected from 48 submissions. They discuss new trends in networking infrastructures, security, services and applications while focusing on virtualization and cloud computing for networks, network programming, software defined networks (SDN) and their security.

The five-volume set LNCS 3980-3984 constitutes the refereed proceedings of the International Conference on Computational Science and Its Applications, ICCSA 2006. The volumes present a total of 664 papers organized according to the five major conference themes: computational methods, algorithms and applications high performance technical computing and networks advanced and emerging applications geometric modelling, graphics and visualization information systems and information technologies. This is Part IV.

Gathers the 12 papers presented during the January 2002 workshop on high performance computing, with an emphasis on low power design and network processing. Among the topics are reducing power with an L0 instruction cache using history-based prediction, tight nonlinear loop timing estimation, multig

This book provides a systematic and comprehensive insight into current sensing techniques. In addition to describing theoretical and practical aspects of current sensing, the author derives practical design guidelines for achieving an optimal performance through a systematic analysis of different circuit principles. Voltage sense amplifiers are also considered, since they are used as a final comparator in a current sense amplifier. Innovative concepts, such as compensation of the bitline multiplexer and auto-power-down, are elucidated. Although the focus is on embedded static random access memory (SRAM), the material presented applies to any current-providing memory type, e.g. also to emerging memory technologies such as MRAM. The book will appeal to design engineers in industry and also to researchers wishing to learn about, and apply, current sensing techniques.

Papers from a January 2002 conference are organized into four sessions each on low power design, synthesis, testing, layout, and interconnects and technology, as well as two sessions each on embedded systems, verification, and VLSI architecture, one session on analog design, and one session on hot c

Wafer-scale integration has long been the dream of system designers. Instead of

chopping a wafer into a few hundred or a few thousand chips, one would just connect the circuits on the entire wafer. What an enormous capability wafer-scale integration would offer: all those millions of circuits connected by high-speed on-chip wires. Unfortunately, the best known optical systems can provide suitably ?ne resolution only over an area much smaller than a whole wafer. There is no known way to pattern a whole wafer with transistors and wires small enough for modern circuits. Statistical defects present a ?rmer barrier to wafer-scale integration. Flaws appear regularly in integrated circuits; the larger the circuit area, the more probable there is a ?aw. If such ?aws were the result only of dust one might reduce their numbers, but ?aws are also the inevitable result of small scale. Each feature on a modern integrated circuit is carved out by only a small number of photons in the lithographic process. Each transistor gets its electrical properties from only a small number of impurity atoms in its tiny area. Inevitably, the quantized nature of light and the atomic nature of matter produce statistical variations in both the number of photons de?ning each tiny shape and the number of atoms providing the electrical behavior of tiny transistors. No known way exists to eliminate such statistical variation, nor may any be possible.

This book provides readers with a variety of algorithms and software tools, dedicated to the physical design of through-silicon-via (TSV) based, three-dimensional integrated circuits. It describes numerous “manufacturing-ready” GDSII-level layouts of TSV-based 3D ICs developed with the tools covered in the book. This book will also feature sign-off level analysis of timing, power, signal integrity, and thermal analysis for 3D IC designs. Full details of the related algorithms will be provided so that the readers will be able not only to grasp the core mechanics of the physical design tools, but also to be able to reproduce and improve upon the results themselves. This book will also offer various design-for-manufacturability (DFM), design-for-reliability (DFR), and design-for-testability (DFT) techniques that are considered critical to the physical design process.