Advanced Fpga Design

The basic concepts and building blocks for the design of Fine- (or FPGA) and Coarse-Grain Reconfigurable Architectures are discussed in this book. Recently-developed integrated architecture design and software-supported design flow of FPGA and coarse-grain reconfigurable architecture are also described.

This book is about the Zynq-7000 All Programmable System on Chip, the family of devices from Xilinx that combines an application-grade ARM Cortex-A9 processor with traditional FPGA logic fabric. Catering for both new and experienced readers, it covers fundamental issues in an accessible way, starting with a clear overview of the device architecture, and an introduction to the design tools and processes for developing a Zynq SoC. Later chapters progress to more advanced topics such as embedded systems development, IP block design and operating systems. Maintaining a 'real-world' perspective, the book also compares Zynq with other device alternatives, and considers end-user applications. The Zynq Book is accompanied by a set of practical tutorials hosted on a companion website. These tutorials will guide the reader through first steps with Zynq, following on to a complete, audio-based embedded systems design.

This book describes best practices for successful

FPGA design. It is the result of the author's meetings with hundreds of customers on the challenges facing each of their FPGA design teams. By gaining an understanding into their design environments, processes, what works and what does not work, key areas of concern in implementing system designs have been identified and a recommended design methodology to overcome these challenges has been developed. This book's content has a strong focus on design teams that are spread across sites. The goal being to increase the productivity of FPGA design teams by establishing a common methodology across design teams; enabling the exchange of design blocks across teams. Coverage includes the complete FPGA design flow, from the basics to advanced techniques. This new edition has been enhanced to include new sections on System modeling, embedded design and high level design. The original sections on Design Environment, RTL design and timing closure have all been expanded to include more up to date techniques as well as providing more extensive scripts and RTL code that can be reused by readers. Presents complete, field-tested methodology for FPGA design, focused on reuse across design teams; Offers best practices for FPGA timing closure, in-system debug, and board design; Details techniques to resolve common pitfalls in designing with FPGAs.

System-on-a-chip (SoC) has become an essential

technique to lower product costs and maximize power efficiency, particularly as the mobility and size requirements of electronics continues to grow. It has therefore become increasingly important for electrical engineers to develop a strong understanding of the key stages of hardware description language (HDL) design flow based on cell-based libraries or field-programmable gate array (FPGA) devices. Honed and revised through years of classroom use, Lin focuses on developing, verifying, and synthesizing designs of practical digital systems using the most widely used hardware description Language: Verilog HDL. Explains how to perform synthesis and verification to achieve optimized synthesis results and compiler times Offers complete coverage of Verilog syntax Illustrates the entire design and verification flow using an FPGA case study Presents real-world design examples such as LED and LCD displays, GPIO, UART, timers, and CPUs Emphasizes design/implementation tradeoff options, with coverage of ASICs and FPGAs Provides an introduction to design for testability Gives readers deeper understanding by using problems and review questions in each chapter Comes with downloadable Verilog HDL source code for most examples in the text Includes presentation slides of all book figures for student reference Digital System Designs and Practices Using Verilog HDL and FPGAs is an ideal

textbook for either fundamental or advanced digital design courses beyond the digital logic design level. Design engineers who want to become more proficient users of Verilog HDL as well as design FPGAs with greater speed and accuracy will find this book indispensable.

This book describes the life cycle process of IP cores, from specification to production, including IP modeling, verification, optimization, and protection. Various trade-offs in the design process are discussed, including those associated with many of the most common memory cores, controller IPs and system-on-chip (SoC) buses. Readers will also benefit from the author's practical coverage of new verification methodologies. such as bug localization, UVM, and scan-chain. A SoC case study is presented to compare traditional verification with the new verification methodologies. Discusses the entire life cycle process of IP cores, from specification to production, including IP modeling, verification, optimization, and protection; Introduce a deep introduction for Verilog for both implementation and verification point of view. Demonstrates how to use IP in applications such as memory controllers and SoC buses. Describes a new verification methodology called bug localization; Presents a novel scan-chain methodology for RTL debugging; Enables readers to employ UVM methodology in straightforward, practical terms.

This textbook teaches students techniques for the design of advanced digital systems using Field Programmable Gate Arrays (FPGAs). The authors focus on communication between FPGAs and peripheral devices (such as EEPROM, analog-to-digital converters, sensors, digital-to-analog converters, displays etc.) and in particular state machines and timed state machines for the implementation of serial communication protocols, such as UART, SPI, I2C, and display protocols, such as VGA, HDMI. VHDL is used as the programming language and all topics are covered in a structured, step-by-step manner.

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This book provides the foundations for understanding hardware security and trust, which have become major concerns for national security over the past decade. Coverage includes issues related to security and trust in a variety of electronic devices and systems related to the security of hardware, firmware and software, spanning system applications, online transactions and networking services. This serves as an invaluable reference to the state-of-the-art research that is of critical significance to the security of and trust in, modern society's microelectronic-supported infrastructures.

The practical guide for every circuit designer creating FPGA designs with Verilog! Walk through design

step-by-step-from coding through silicon. Partitioning, synthesis, simulation, test benches, combinatorial and sequential designs, and more. Real World FPGA Design with Verilog guides you through every key challenge associated with designing FPGAs and ASICs using Verilog, one of the world's leading hardware design languages. You'll find irreverent, yet rigorous coverage of what it really takes to translate HDL code into hardware-and how to avoid the pitfalls that can occur along the way. Ken Coffman presents no-frills, real-world design techniques that can improve the stability and reliability of virtually any design. Start by walking a typical Verilog design all the way through to silicon; then, review basic Verilog syntax, design; simulation and testing, advanced simulation, and more. Coverage includes: Essential digital design strategies: recognizing the underlying analog building blocks used to create digital primitives; implementing logic with LUTs; clocking strategies, logic minimization, and more Key engineering tradeoffs, including operating speed vs. latency Combinatorial and sequential designs Verilog test fixtures: compiler directives and automated testing A detailed comparison of alternative architectures and software-including a never-before-published FPGA technology selection checklist Real World FPGA Design with Verilog introduces libraries and reusable modules, points out opportunities to reuse your own

code, and helps you decide when to purchase existing IP designs instead of building from scratch. Essential rules for designing with ASIC conversion in mind are presented. If you're involved with digital hardware design with Verilog, Ken Coffman is a welcome voice of experience-showing you the shortcuts, helping you over the rough spots, and helping you achieve competence faster than you ever expected!

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This book collects the best practices FPGA-based Prototyping of SoC and ASIC devices into one place for the first time, drawing upon not only the authors' own knowledge but also from leading practitioners worldwide in order to present a snapshot of best practices today and possibilities for the future. The book is organized into chapters which appear in the same order as the tasks and decisions which are performed during an FPGA-based prototyping project. We start by analyzing the challenges and benefits of FPGA-based Prototyping and how they compare to other prototyping methods. We present the current state of the available FPGA technology and tools and how to get started on a project. The FPMM also compares between home-made and outsourced FPGA platforms and how to analyze which will best meet the needs of a given project. The central chapters deal with implementing an SoC design in FPGA technology including clocking,

conversion of memory, partitioning, multiplexing and handling IP amongst many other subjects. The important subject of bringing up the design on the FPGA boards is covered next, including the introduction of the real design into the board, running embedded software upon it in and debugging and iterating in a lab environment. Finally we explore how the FPGA-based Prototype can be linked into other verification methodologies, including RTL simulation and virtual models in SystemC. Along the way, the reader will discover that an adoption of FPGA-based Prototyping from the beginning of a project, and an approach we call Design-for-Prototyping, will greatly increase the success of the prototype and the whole SoC project, especially the embedded software portion. Design-for-Prototyping is introduced and explained and promoted as a manifesto for better SoC design. Readers can approach the subjects from a number of directions. Some will be experienced with many of the tasks involved in FPGA-based Prototyping but are looking for new insights and ideas; others will be relatively new to the subject but experienced in other verification methodologies; still others may be project leaders who need to understand if and how the benefits of FPGA-based prototyping apply to their next SoC project. We have tried to make each subject chapter relatively standalone, or where necessary, make numerous forward and backward

references between subjects, and provide recaps of certain key subjects. We hope you like the book and we look forward to seeing you on the FPMM on-line community soon (go to www.synopsys.com/fpmm).
This book describes RTL design using Verilog, synthesis and timing closure for System On Chip (SOC) design blocks. It covers the complex RTL design scenarios and challenges for SOC designs and provides practical information on performance improvements in SOC, as well as Application Specific Integrated Circuit (ASIC) designs. Prototyping using modern high density Field Programmable Gate Arrays (FPGAs) is discussed in this book with the practical examples and case studies. The book discusses SOC design, performance improvement techniques, testing and system level verification, while also describing the modern Intel FPGA/XILINX FPGA architectures and their use in SOC prototyping. Further, the book covers the Synopsys Design Compiler (DC) and Prime Time (PT) commands, and how they can be used to optimize complex ASIC/SOC designs. The contents of this book will be useful to students and professionals alike.
SystemVerilog provides abundant features that could overwhelm a SystemVerilog beginner. Fortunately, for a decent RTL design, only a small subset of SystemVerilog is needed. The purpose of this book is to carefully choose the right subset of

SystemVerilog so that the digital designer can comfortably start their SystemVerilog design project. In this book, FPGA application is chosen not only for its easy and quick practice but also for its wider adoption. SystemVerilog examples will be deployed broadly throughout this book for reference. For those who want to learn HDL design, this book will help them ramp up their HDL design skill quickly while avoiding the pitfalls. For those who have experience in Verilog but want to advance their knowledge to SystemVerilog, this book can be a good reference. For the VHDL designers who want to explore the features in SystemVerilog, this book can serve as a bridge since it is written in a way that the common and different concepts between VHDL and SystemVerilog are emphasized.The following are the specialties of this book:1. It provides a carefully chosen subset of SystemVerilog language for FPGA design.2. It provides a great number of examples for easier learning and practice3. It shows using SystemVerilog as an efficient way for a productive verification4. It emphasizes on the FPGA application but the presented RTL design is also applicable to ASIC.This book is organized as follows: Chapter 1 first briefly describes the HDL digital design methodology. Then it describes SystemVerilog language and its syntax. The basic topics include lexical convention, data type, operators, and expressions. It also explains various programming

statements such as assignment statements, if-else statements, case statements and loop statements.Chapter 2 shows how to use SystemVerilog to describe the basic digital gates and digital hardware circuits as well as to model their behavior. It explains SytemVerilog modelling constructs. The constructs are modules, procedures, interfaces, functions and packages. This chapter also covers advanced topics such as compiler directives, digital arithmetic operation and design optimization.Chapter 3 introduces the synchronous sequential digital design. It gives some example designs such as flip-flop registers, shift registers, counters and adders. The design of finite-state machine (FSM) is discussed in depth for control circuit in digital systems. The algorithmic state machine (ASM) with data path is described for data-processing digital system. It also addresses other advanced topics of timing analysis, design performance and clock-domain crossing.Chapter 4 focuses on the functional simulation of digital design. It describes the general construction of test bench using SystemVerilog. It introduces the initial procedure for pre-simulation initialization, the final procedure for post-simulation processing and the task procedure for repetitive operations. It explains how to control the simulation proceeding with procedure timing control. It presents some useful system functions and tasks for math functions, file

I/O and etc.. Chapter 5 addresses the FPGA design methodology. The topics covers design flow, design environment, intellectual property (IP) core usage, simulation and constraints. The FPGA design for system-on-chip (SOC) is emphasized as this type of FPGA becomes popular. The FPGA configuration options are discussed. Last but not least, it introduces helpful FPGA design practices for a successful design.

Design Recipes for FPGAs: Using Verilog and VHDL provides a rich toolbox of design techniques and templates to solve practical, every-day problems using FPGAs. Using a modular structure, the book gives ‘easy-to-find’ design techniques and templates at all levels, together with functional code. Written in an informal and ‘easy-to-grasp’ style, it goes beyond the principles of FPGA s and hardware description languages to actually demonstrate how specific designs can be synthesized, simulated and downloaded onto an FPGA. This book's ‘easy-to-find’ structure begins with a design application to demonstrate the key building blocks of FPGA design and how to connect them, enabling the experienced FPGA designer to quickly select the right design for their application, while providing the less experienced a ‘road map’ to solving their specific design problem. The book also provides advanced techniques to create ‘real world’ designs that fit the device required and which are fast and reliable to

implement. This text will appeal to FPGA designers of all levels of experience. It is also an ideal resource for embedded system development engineers, hardware and software engineers, and undergraduates and postgraduates studying an embedded system which focuses on FPGA design. A rich toolbox of practical FGPA design techniques at an engineer's finger tips Easy-to-find structure that allows the engineer to quickly locate the information to solve their FGPA design problem, and obtain the level of detail and understanding needed

Master the art of FPGA digital system design with Verilog and VHDL This practical guide offers comprehensive coverage of FPGA programming using the two most popular hardware description languages—Verilog and VHDL. You will expand your marketable electronic design skills and learn to fully utilize FPGA programming concepts and techniques. Digital System Design with FPGA: Implementation Using Verilog and VHDL begins with basic digital design methods and continues, step-by-step, to advanced topics, providing a solid foundation that allows you to fully grasp the core concepts. Real-life examples, start-to-finish projects, and ready-to-run Verilog and VHDL code is provided throughout. • Concepts are explained using two affordable boards—the Basys 3 and Arty • Includes PowerPoint slides, downloadable figures, and an instructor's solutions manual • Written by a pair of experienced

electronics designers and instructors

Advanced FPGA DesignArchitecture, Implementation, and OptimizationJohn Wiley & Sons

This book provides the advanced issues of FPGA design as the underlying theme of the work. In practice, an engineer typically needs to be mentored for several years before these principles are appropriately utilized. The topics that will be discussed in this book are essential to designing FPGA's beyond moderate complexity. The goal of the book is to present practical design techniques that are otherwise only available through mentorship and real-world experience.

This book is designed to serve as a hands-on professional reference with additional utility as a textbook for upper undergraduate and some graduate courses in digital logic design. This book is organized in such a way that that it can describe a number of RTL design scenarios, from simple to complex. The book constructs the logic design story from the fundamentals of logic design to advanced RTL design concepts. Keeping in view the importance of miniaturization today, the book gives practical information on the issues with ASIC RTL design and how to overcome these concerns. It clearly explains how to write an efficient RTL code and how to improve design performance. The book also describes advanced RTL design concepts such as low-power design, multiple clock-domain design, and SOC-based design. The practical orientation of the book makes it ideal for training programs for practicing design engineers and for short-term vocational programs. The contents of the book will also make it a useful read for students and hobbyists.

The methodology described in this book is the result of many years of research experience in the field of synthesizable VHDL design targeting FPGA based platforms. VHDL was first conceived as a documentation language for ASIC

designs. Afterwards, the language was used for the behavioral simulation of ASICs, and also as a design input for synthesis tools. VHDL is a rich language, but just a small subset of it can be used to write synthesizable code, from which a physical circuit can be obtained. Usually VHDL books describe both, synthesis and simulation aspects of the language, but in this book the reader is conducted just through the features acceptable by synthesis tools. The book introduces the subjects in a gradual and concise way, providing just enough information for the reader to develop their synthesizable digital systems in VHDL. The examples in the book were planned targeting an FPGA platform widely used around the world.

Dr Donald Bailey starts with introductory material considering the problem of embedded image processing, and how some of the issues may be solved using parallel hardware solutions. Field programmable gate arrays (FPGAs) are introduced as a technology that provides flexible, fine-grained hardware that can readily exploit parallelism within many image processing algorithms. A brief review of FPGA programming languages provides the link between a software mindset normally associated with image processing algorithms, and the hardware mindset required for efficient utilization of a parallel hardware design. The design process for implementing an image processing algorithm on an FPGA is compared with that for a conventional software implementation, with the key differences highlighted. Particular attention is given to the techniques for mapping an algorithm onto an FPGA implementation, considering timing, memory bandwidth and resource constraints, and efficient hardware computational techniques. Extensive coverage is given of a range of low and intermediate level image processing operations, discussing efficient implementations and how these may vary according to the application. The

techniques are illustrated with several example applications or case studies from projects or applications he has been involved with. Issues such as interfacing between the FPGA and peripheral devices are covered briefly, as is designing the system in such a way that it can be more readily debugged and tuned. Provides a bridge between algorithms and hardware Demonstrates how to avoid many of the potential pitfalls Offers practical recommendations and solutions Illustrates several real-world applications and case studies Allows those with software backgrounds to understand efficient hardware implementation Design for Embedded Image Processing on FPGAs is ideal for researchers and engineers in the vision or image processing industry, who are looking at smart sensors, machine vision, and robotic vision, as well as FPGA developers and application engineers. The book can also be used by graduate students studying imaging systems, computer engineering, digital design, circuit design, or computer science. It can also be used as supplementary text for courses in advanced digital design, algorithm and hardware implementation, and digital signal processing and applications. Companion website for the book: www.wiley.com/go/bailey/fpga

This book constitutes the refereed proceedings of the 8th International Workshop on Field-Programmable Logics and Applications, FPL '98, held in Tallinn, Estonia, in August/September 1998. The 39 revised full papers presented were carefully selected for inclusion in the book from a total of 86 submissions. Also included are 30 refereed high-quality posters. The papers are organized in topical sections on design methods, general aspects, prototyping and simulation, development methods, accelerators, system architectures, hardware/software codesign, system development, algorithms on FPGAs, and applications.

Annotation Deploy and optimize your wireless LAN using the

new standard for broadband wireless communication, OFDM. A comprehensive reference written by two experts who helped create the OFDM specifications. A detailed, practical guide to OFDM WLANs does not exist, requiring readers to seek out multiple sources of information, such as white papers and research notes. Detailed explanations of the concepts and algorithms behind OFDM-context that is missing from the two OFDM books currently available. This book explains OFDM WLAN basics, including components of OFDM and multicarrier WLAN standards. It provides a practical approach to OFDM by including software and hardware examples and detailed implementation explanations. OFDM Multicarrier Wireless Networks: A Practical Approach defines and explains the mathematical concepts behind OFDM necessary for successful OFDM WLAN implementations. Juha Heiskala is a research engineer at Nokia Research Center in Irving, TX. Heiskala is active in the IEEE 802.11 standards bodies and has been tasked with developing the 802.11a system simulation on several software platforms. He is the inventor/co-inventor of three pending patents in the area of OFDM LANs and co-designed with Dr. John Terry the modulation and coding scheme for achieving 100 Mbps speeds within currently allocated band specifications for OFDM WLANs. John Terry, Ph.D. is a senior research engineer at Nokia Research Center. He is currently managing the OFDM modulation and coding project in the HSA group. Dr. Terry has published several white papers, given numerous presentations on wireless communications, and generated four patents related to OFDM WLANs. He has 10 years of experience working in wireless communications, including tenures at NASA Glen Research Center and Texas Instruments.

In August of 2006, an engineering VP from one of Altera’s customers approached Misha Burich, VP of Engineering at

Altera, asking for help in reliably being able to predict the cost, schedule and quality of system designs reliant on FPGA designs. At this time, I was responsible for defining the design flow requirements for the Altera design software and was tasked with investigating this further. As I worked with the customer to understand what worked and what did not work reliably in their FPGA design process, I noted that this problem was not unique to this one customer. The characteristics of the problem are shared by many Corporations that implement designs in FPGAs. The Corporation has many design teams at different locations and the success of the FPGA projects vary between the teams. There is a wide range of design experience across the teams. There is no working process for sharing design blocks between engineering teams. As I analyzed the data that I had received from hundreds of customer visits in the past, I noticed that design reuse among engineering teams was a challenge. I also noticed that many of the design teams at the same Companies and even within the same design team used different design methodologies. Altera had recently solved this problem as part of its own FPGA design software and IP development process.

A hands-on introduction to FPGA prototyping and SoC design This Second Edition of the popular book follows the same “learning-by-doing” approach to teach the fundamentals and practices of VHDL synthesis and FPGA prototyping. It uses a coherent series of examples to demonstrate the process to develop sophisticated digital circuits and IP (intellectual property) cores, integrate them into an SoC (system on a chip) framework, realize the system on an FPGA prototyping board, and verify the hardware and software operation. The examples start with simple gate-level circuits, progress gradually through the RT (register transfer) level modules, and lead to a functional embedded system with custom I/O

peripherals and hardware accelerators. Although it is an introductory text, the examples are developed in a rigorous manner, and the derivations follow strict design guidelines and coding practices used for large, complex digital systems. The new edition is completely updated. It presents the hardware design in the SoC context and introduces the hardware-software co-design concept. Instead of treating examples as isolated entities, the book integrates them into a single coherent SoC platform that allows readers to explore both hardware and software “programmability” and develop complex and interesting embedded system projects. The revised edition: Adds four general-purpose IP cores, which are multi-channel PWM (pulse width modulation) controller, I2C controller, SPI controller, and XADC (Xilinx analog-to-digital converter) controller. Introduces a music synthesizer constructed with a DDFS (direct digital frequency synthesis) module and an ADSR (attack-decay-sustain-release) envelop generator. Expands the original video controller into a complete stream-based video subsystem that incorporates a video synchronization circuit, a test pattern generator, an OSD (on-screen display) controller, a sprite generator, and a frame buffer. Introduces basic concepts of software-hardware co-design with Xilinx MicroBlaze MCS soft-core processor. Provides an overview of bus interconnect and interface circuit. Introduces basic embedded system software development. Suggests additional modules and peripherals for interesting and challenging projects. The FPGA Prototyping by VHDL Examples, Second Edition makes a natural companion text for introductory and advanced digital design courses and embedded system course. It also serves as an ideal self-teaching guide for practicing engineers who wish to learn more about this emerging area of interest.

In 1998-99, at the dawn of the SoC Revolution, we wrote

Surviving the SOC Revolution: A Guide to Platform Based Design. In that book, we focused on presenting guidelines and best practices to aid engineers beginning to design complex System-on-Chip devices (SoCs). Now, in 2003, facing the mid-point of that revolution, we believe that it is time to focus on winning. In this book, Winning the SoC Revolution: Experiences in Real Design, we gather the best practical experiences in how to design SoCs from the most advanced design groups, while setting the issues and techniques in the context of SoC design methodologies. As an edited volume, this book has contributions from the leading design houses who are winning in SoCs - Altera, ARM, IBM, Philips, TI, UC Berkeley, and Xilinx. These chapters present the many facets of SoC design - the platform based approach, how to best utilize IP, Verification, FPGA fabrics as an alternative to ASICs, and next generation process technology issues. We also include observations from Ron Wilson of CMP Media on best practices for SoC design team collaboration. We hope that by utilizing this book, you too, will win the SoC Revolution.

CD-ROM contains: Silos-III Verilog desgn environment and simulator -- Kilinx integrated synthesis environment (ISE) synthesis tool for FPGAs.

Get started with FPGA programming using SystemVerilog, and develop real-world skills by building projects, including a calculator and a keyboard Key Features Explore different FPGA usage methods and the FPGA tool flow Learn how to design, test, and implement hardware circuits using SystemVerilog Build real-world FPGA projects such as a calculator and a keyboard

using FPGA resources Book Description Field Programmable Gate Arrays (FPGAs) have now become a core part of most modern electronic and computer systems. However, to implement your ideas in the real world, you need to get your head around the FPGA architecture, its toolset, and critical design considerations. FPGA Programming for Beginners will help you bring your ideas to life by guiding you through the entire process of programming FPGAs and designing hardware circuits using SystemVerilog. The book will introduce you to the FPGA and Xilinx architectures and show you how to work on your first project, which includes toggling an LED. You'll then cover SystemVerilog RTL designs and their implementations. Next, you'll get to grips with using the combinational Boolean logic design and work on several projects, such as creating a calculator and updating it using FPGA resources. Later, the book will take you through the advanced concepts of AXI and serial interfaces and show you how to create a keyboard using PS/2. Finally, you'll be able to consolidate all the projects in the book to create a unified output using a Video Graphics Array (VGA) controller that you'll design. By the end of this SystemVerilog FPGA book, you'll have learned how to work with FPGA systems and be able to design hardware circuits and boards using SystemVerilog programming. What you will learn Understand the FPGA architecture and its implementation Get to grips with writing SystemVerilog RTL Make FPGA projects using SystemVerilog programming Work with computer math basics, parallelism, and pipelining Explore the advanced

topics of AXI and serial interfaces Discover how you can implement a VGA interface in your projects Who this book is for This FPGA design book is for embedded system developers, engineers, and programmers who want to learn FPGA and SystemVerilog programming from scratch. FPGA designers looking to gain hands-on experience in working on real-world projects will also find this book useful.

This book describes the optimized implementations of several arithmetic datapath, controlpath and pseudorandom sequence generator circuits for realization of high performance arithmetic circuits targeted towards a specific family of the high-end Field Programmable Gate Arrays (FPGAs). It explores regular, modular, cascadable and bit-sliced architectures of these circuits, by directly instantiating the target FPGA-specific primitives in the HDL. Every proposed architecture is justified with detailed mathematical analyses. Simultaneously, constrained placement of the circuit building blocks is performed, by placing the logically related hardware primitives in close proximity to one another by supplying relevant placement constraints in the Xilinx proprietary “User Constraints File”. The book covers the implementation of a GUI-based CAD tool named FlexiCore integrated with the Xilinx Integrated Software Environment (ISE) for design automation of platform-specific high-performance arithmetic circuits from user-level specifications. This tool has been used to implement the proposed circuits, as well as hardware implementations of integer arithmetic algorithms where several of the proposed circuits are used as building

blocks. Implementation results demonstrate higher performance and superior operand-width scalability for the proposed circuits, with respect to implementations derived through other existing approaches. This book will prove useful to researchers, students and professionals engaged in the domain of FPGA circuit optimization and implementation.

The push to move products to market as quickly and cheaply as possible is fiercer than ever, and accordingly, engineers are always looking for new ways to provide their companies with the edge over the competition. Field-Programmable Gate Arrays (FPGAs), which are faster, denser, and more cost-effective than traditional programmable logic devices (PLDs), are quickly becoming one of the most widespread tools that embedded engineers can utilize in order to gain that needed edge. FPGAs are especially popular for prototyping designs, due to their superior speed and efficiency. This book hones in on that rapid prototyping aspect of FPGA use, showing designers exactly how they can cut time off production cycles and save their companies money drained by costly mistakes, via prototyping designs with FPGAs first. Reading it will take a designer with a basic knowledge of implementing FPGAs to the “next-level of FPGA use because unlike broad beginner books on FPGAs, this book presents the required design skills in a focused, practical, example-oriented manner. In-the-trenches expert authors assure the most applicable advice to practicing engineers Dual focus on successfully making critical decisions and avoiding common pitfalls appeals to engineers pressured

for speed and perfection Hardware and software are both covered, in order to address the growing trend toward "cross-pollination" of engineering expertise ??????????????????,??????????????,????????????????,???????????

This comprehensive textbook on the field programmable gate array (FPGA) covers its history, fundamental knowledge, architectures, device technologies, computer-aided design technologies, design tools, examples of application, and future trends. Programmable logic devices represented by FPGAs have been rapidly developed in recent years and have become key electronic devices used in most IT products. This book provides both complete introductions suitable for students and beginners, and high-level techniques useful for engineers and researchers in this field. Differently developed from usual integrated circuits, the FPGA has unique structures, design methodologies, and application techniques. Allowing programming by users, the device can dramatically reduce the rising cost of development in advanced semiconductor chips. The FPGA is now driving the most advanced semiconductor processes and is an all-in-one platform combining memory, CPUs, and various peripheral interfaces. This book introduces the FPGA from various aspects for readers of different levels. Novice learners can acquire a fundamental knowledge of the FPGA, including its history, from Chapter 1; the first half of Chapter 2; and Chapter 4. Professionals who are already familiar with the device will gain a deeper understanding of the structures and design methodologies from Chapters 3 and 5. Chapters

6–8 also provide advanced techniques and cutting-edge applications and trends useful for professionals. Although the first parts are mainly suitable for students, the advanced sections of the book will be valuable for professionals in acquiring an in-depth understanding of the FPGA to maximize the performance of the device. This book describes best practices for successful FPGA design. It is the result of the author's meetings with hundreds of customers on the challenges facing each of their FPGA design teams. By gaining an understanding into their design environments, processes, what works and what does not work, key areas of concern in implementing system designs have been identified and a recommended design methodology to overcome these challenges has been developed. This book's content has a strong focus on design teams that are spread across sites. The goal being to increase the productivity of FPGA design teams by establishing a common methodology across design teams; enabling the exchange of design blocks across teams. Coverage includes the complete FPGA design flow, from the basics to advanced techniques. This new edition has been enhanced to include new sections on System modeling, embedded design and high level design. The original sections on Design Environment, RTL design and timing closure have all been expanded to include more up to date techniques as well as providing more extensive scripts and RTL code that can be reused by readers. Presents complete, field-tested methodology for FPGA design, focused on reuse across design teams; Offers best practices for FPGA timing closure, in-system debug,

and board design; Details techniques to resolve common pitfalls in designing with FPGAs.

This book presents the methodologies and for embedded systems design, using field programmable gate array (FPGA) devices, for the most modern applications. Coverage includes state-of-the-art research from academia and industry on a wide range of topics, including applications, advanced electronic design automation (EDA), novel system architectures, embedded processors, arithmetic, and dynamic reconfiguration.

Field programmable gate array (FPGAs) belong to the family of programmable logic devices and designing with FPGAs require knowledge of digital design. The book begins with an overview of boolean algebra and logic design followed by topics on programmable logic devices. Introduction to field programmable devices is then explained right from the basic FPGA which was used as glue logic to present day very advanced FPGA used in Embedded Systems including military and space applications. Further, it goes on to discuss the evolution of Xilinx, Altera/Intel and Actel/Microsemi FPGAs and their architectural features, and includes many design examples in VHDL and a brief introduction to System Verilog. The last three chapters discuss the Xilinx FPGA design flow completely from architectural specification to obtaining a bit stream to be loaded into the FPGA.

Testing methodologies and design exercises using Spartan Series and the important research issues of FPGA Security along with the Future of FPGAs for the next two decades are described as well.

Start by walking a typical Verilog design all the way through to silicon; then, review basic Verilog syntax, design, simulation and testing, advanced simulation, and more."--BOOK JACKET.

This book covers basic fundamentals of logic design and advanced RTL design concepts using VHDL. The book is organized to describe both simple and complex RTL design scenarios using VHDL. It gives practical information on the issues in ASIC prototyping using FPGAs, design challenges and how to overcome practical issues and concerns. It describes how to write an efficient RTL code using VHDL and how to improve the design performance. The design guidelines by using VHDL are also explained with the practical examples in this book. The book also covers the ALTERA and XILINX FPGA architecture and the design flow for the PLDs. The contents of this book will be useful to students, researchers, and professionals working in hardware design and optimization. The book can also be used as a text for graduate and professional development courses.

FPGAs are enabling more applications to be put to the market at a fraction of the cost of ASICs and with a much faster deployment rate. However, the wide

range of FPGA brands and types currently available on the market; could overwhelm first time users when choosing a suitable FPGA for a given application. Furthermore, intermediate-to-advanced FPGA users may desire to evaluate some new FPGAs before committing to a purchase. FPGA to the Cloud is a web application that allows users to interact with FPGA evaluation kits remotely on a try-before-you-buy or pay-per-use model. The end user would access a web site where the web application is hosted. The end user would select an FPGA evaluation board from a list, and would be given direct remote access to said FPGA board; with programming tools. The user could use available sample FPGA design files, or upload user-created FPGA design files; for testing and evaluation. The project-prototype is based on the ZedBoard which uses Xilinx's Zynq-7000 FPGA. The web application was developed using Laravel's PHP framework.